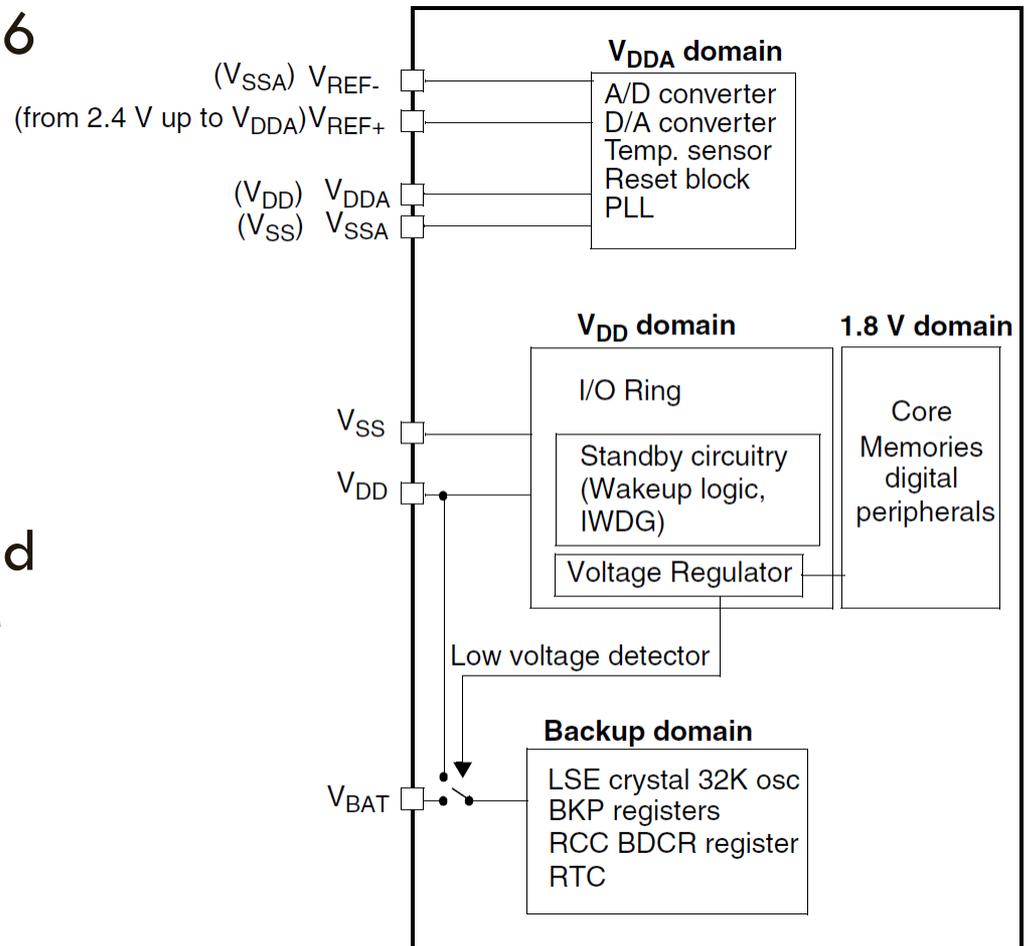




STM32 MICROCONTROLLER

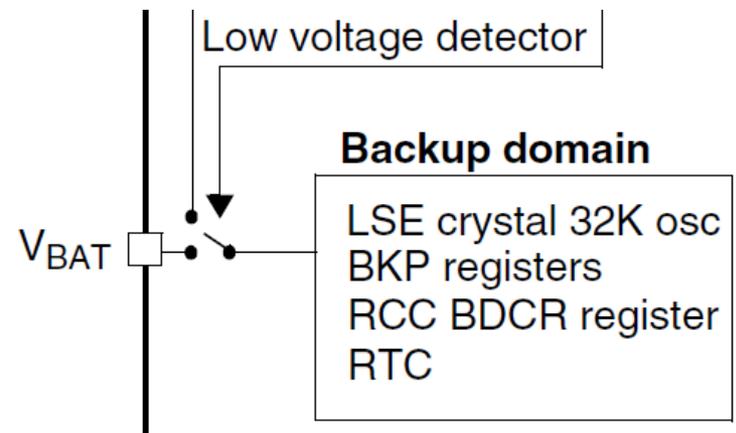
Power Supplies

- Device requires a 2.0:3.6 V operating voltage supply (VDD)
- Embedded regulator is used to supply the internal 1.8 V digital power
- Real-time clock (RTC) and backup registers can be powered from VBAT voltage when main VDD supply is powered off



Battery Backup Domain

- To retain the content of the Backup registers and supply the RTC function when VDD is turned off, VBAT pin can be connected to an optional standby voltage supplied by a battery or by another source
 - ▣ The VBAT pin powers the RTC unit, the LSE oscillator and the PC13 to PC15 IOs, allowing the RTC to operate even when the main digital supply (VDD) is turned off
- The switch to the VBAT supply is controlled by the Power Down Reset embedded in the Reset block

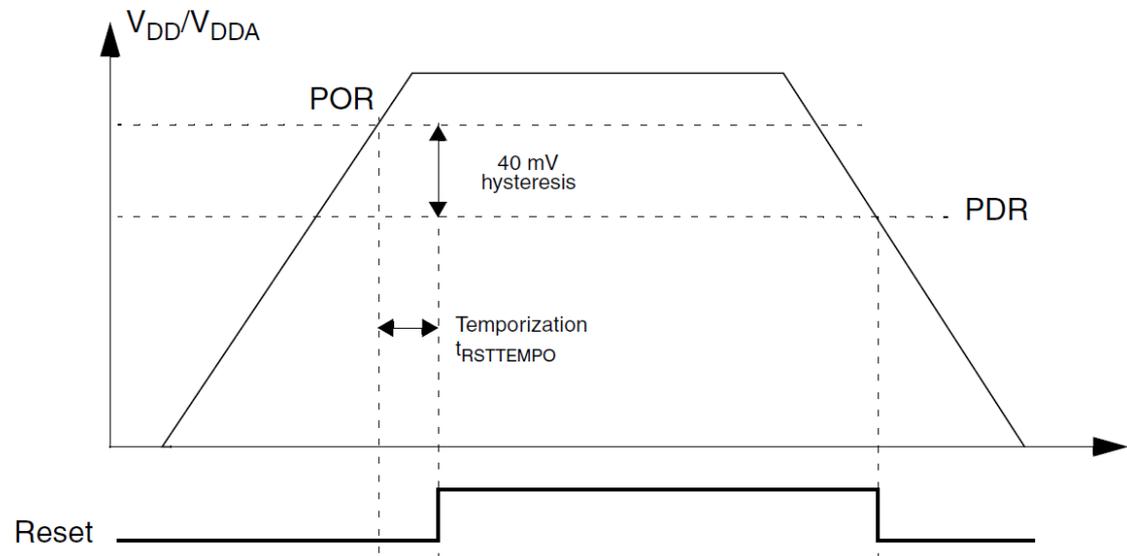


Voltage Regulator

- The voltage regulator is always enabled after Reset and works in three different modes depending on the application modes:
 - ▣ **Run mode:** the regulator supplies full power to the 1.8 V domain (core, memories and digital peripherals)
 - ▣ **Stop mode:** the regulator supplies low-power to the 1.8 V domain, preserving contents of registers and SRAM
 - ▣ **Standby Mode:** the regulator is powered off. The contents of the registers and SRAM are lost except for the Standby circuitry and the Backup Domain

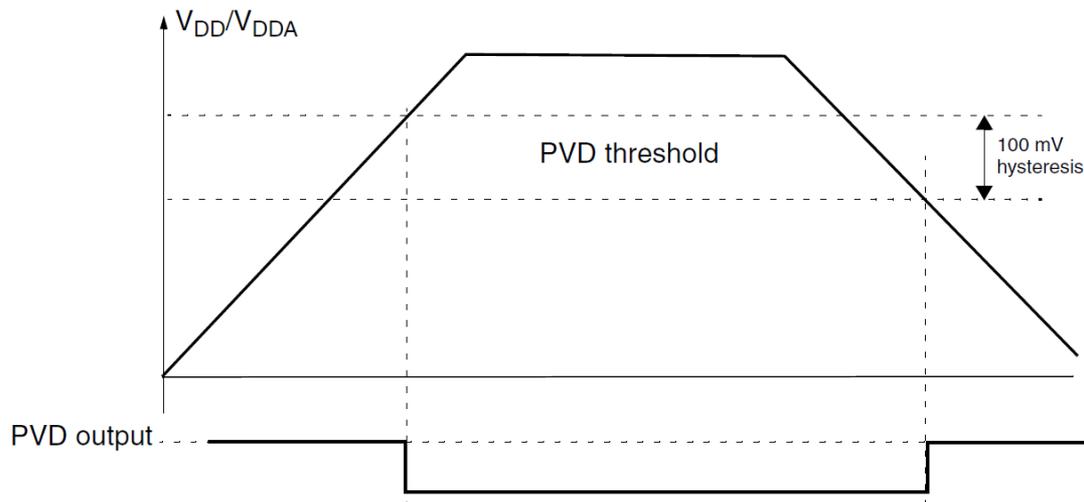
Power Supply Supervisor

- Power on reset (POR)/power down reset (PDR)
 - ▣ Integrated POR/PDR circuitry that allows proper operation starting from/down to 2 V
 - ▣ Device remains in Reset mode when V_{DD}/V_{DDA} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit



Power Supply Supervisor

- Programmable voltage detector (PVD)
 - ▣ Monitors the V_{DD}/V_{DDA} power supply by comparing it to a threshold selected by the PLS[2:0] bits in the *Power control register (PWR_CR)*
 - ▣ PVD is enabled by setting the PVDE bit
 - ▣ A PVDO flag is available, in *Power control/status register (PWR_CSR)*, to indicate if V_{DD}/V_{DDA} is higher or lower than the PVD threshold
 - ▣ This event is internally connected to EXTI and can generate interrupt



Low-Power Modes

- By default, microcontroller is in Run mode after a Reset
- Low power modes are available to save power when the CPU need not to be kept running (e.g., while waiting for an external event)
- It is up to the user to select the mode that gives the best compromise between low-power consumption, short startup time and available wakeup sources.
- The STM32F100xx devices feature three low-power modes:
 - ▣ Sleep mode (CPU clock off, all peripherals including Cortex-M3 core peripherals like NVIC, SysTick, etc. are kept running)
 - ▣ Stop mode (all clocks are stopped)
 - ▣ Standby mode (1.8V domain powered-off)
- In addition, power consumption in Run mode can be reduced by:
 - ▣ Slowing down the system clocks
 - ▣ Gating the clocks to the APB and AHB peripherals when they are unused.

Low-Power Modes

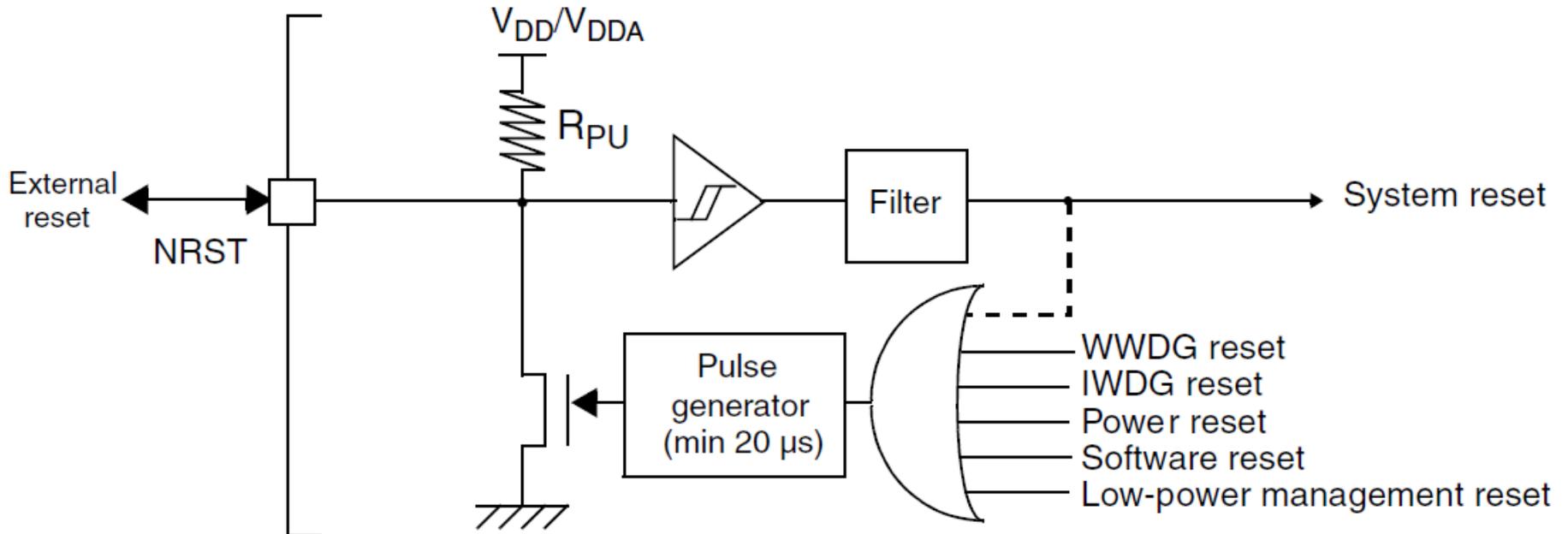
Mode name	Entry	wakeup	Effect on 1.8V domain clocks	Effect on V _{DD} domain clocks	Voltage regulator
Sleep (Sleep now or Sleep-on - exit)	WFI	Any interrupt	CPU clock OFF no effect on other clocks or analog clock sources	None	ON
	WFE	Wakeup event			
Stop	PDDS and LPDS bits + SLEEPDEEP bit + WFI or WFE	Any EXTI line (configured in the EXTI registers)	All 1.8V domain clocks OFF	HSI and HSE oscillators OFF	ON or in low-power mode (depends on <i>Power control register (PWR_CR)</i>)
Standby	PDDS bit + SLEEPDEEP bit + WFI or WFE	WKUP pin rising edge, RTC alarm, external reset in NRST pin, IWDG reset			OFF

Backup Registers (BKP)

- Backup registers are ten 16-bit registers in low and medium density devices for storing 20 bytes of user application data
- They are implemented in the backup domain that remains powered on by VBAT when the VDD power is switched off.
 - ▣ They are not reset when the device wakes up from Standby mode or by a system reset or power reset
- In addition, the BKP control registers are used to manage the Tamper detection feature and RTC calibration.
- After reset, access to the Backup registers and RTC is disabled and the Backup domain (BKP) is protected against possible parasitic write access
- To enable access to the Backup registers and the RTC, proceed as follows:
 - ▣ Enable the power and backup interface clocks by setting the PWREN and BKPEN bits in the RCC_APB1ENR register
 - ▣ Set the DBP bit the Power Control Register (PWR_CR) to enable access to the Backup registers and RTC.

Reset

- There are three types of reset:
 - ▣ System Reset
 - ▣ Power Reset
 - ▣ Backup domain reset



System Reset

- A system reset sets all registers to their reset values except the reset flags in the clock controller CSR register and the registers in the Backup domain
- A system reset is generated when one of the following events occurs:
 - ▣ Low level on the NRST pin (external reset)
 - ▣ Window watchdog end of count condition (WWDG reset)
 - ▣ Independent watchdog end of count condition (IWDG reset)
 - ▣ Software reset (SW reset)
 - ▣ Low-power management reset

System Reset

- Software reset
 - ▣ The SYSRESETREQ bit in Cortex™-M3 Application Interrupt and Reset Control Register must be set to force a software reset on the device
- Low-power management reset:
 - ▣ *Method 1: Reset generated when entering Standby mode:* This type of reset is enabled by resetting nRST_STDBY bit in User Option Bytes. In this case, whenever a Standby mode entry sequence is successfully executed, the device is reset instead of entering Standby mode.
 - ▣ *Method 2: Reset when entering Stop mode:* This type of reset is enabled by resetting NRST_STOP bit in User Option Bytes. In this case, whenever a Stop mode entry sequence is successfully executed, the device is reset instead of entering Stop mode.

Power Reset

- A power reset is generated when one of the following occurs:
 - ▣ Power-on/power-down reset (POR/PDR reset)
 - ▣ When exiting Standby mode
- A power reset sets all registers to their reset values except the Backup domain
 - ▣ These sources act on the NRST pin and it is always kept low during the delay phase. The
 - ▣ RESET vector is fixed at address 0x00000004 in the memory map

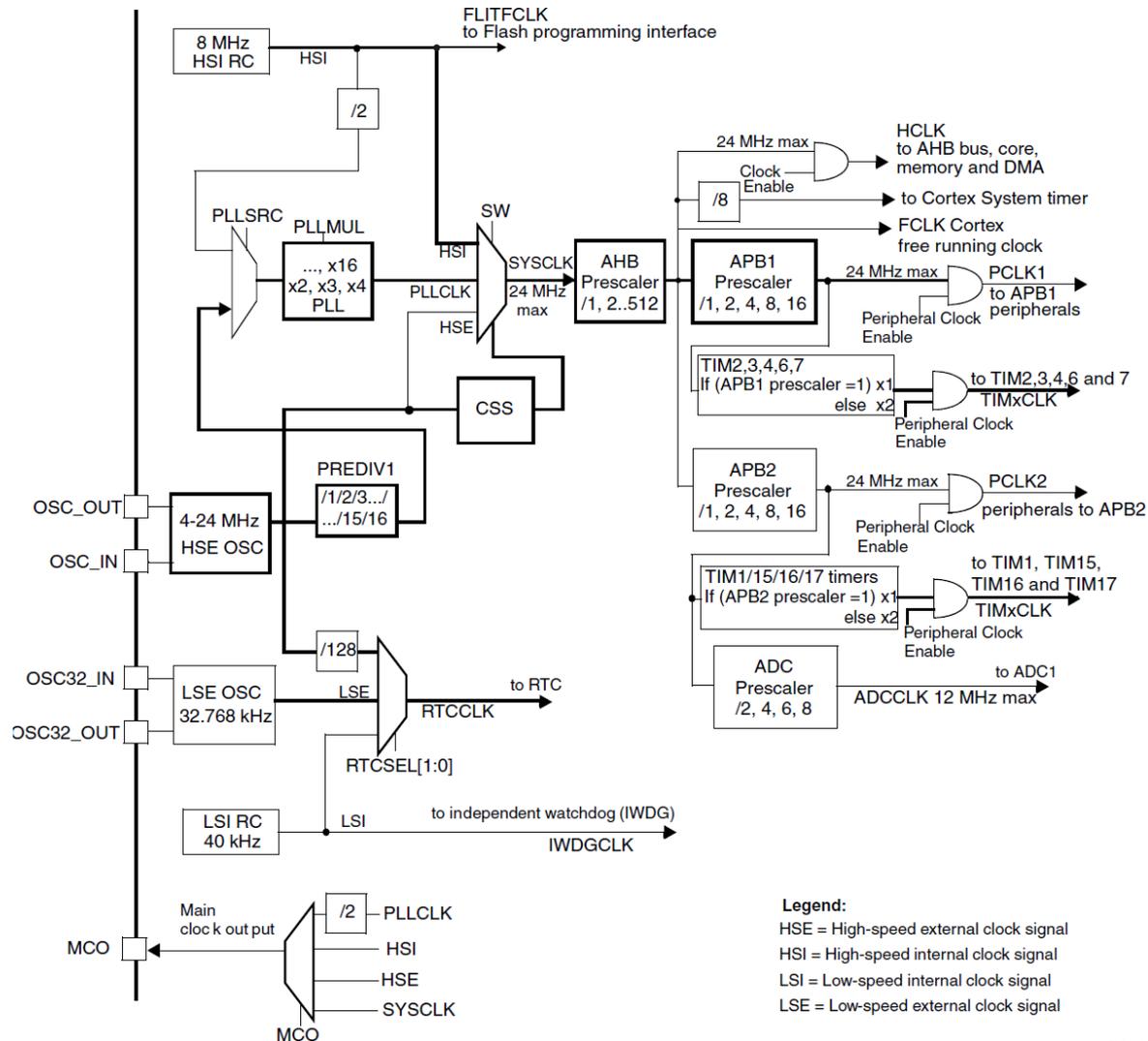
Backup Domain Reset

- Backup domain has two specific resets that affect only the backup domain
- backup domain reset is generated when one of the following events occurs:
 - ▣ Software reset, triggered by setting the BDRST bit in the *Backup domain control register (RCC_BDCR)*
 - ▣ VDD or VBAT power on, if both have previously been powered off

Clocks

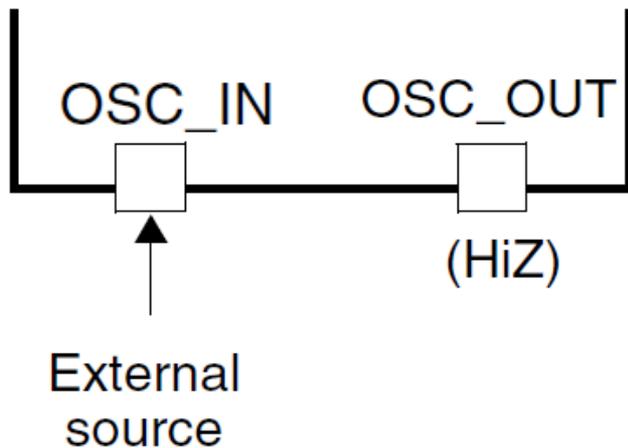
- Three different clock sources can be used to drive the system clock (SYSCLK):
 - ▣ HSI oscillator clock
 - ▣ HSE oscillator clock
 - ▣ PLL clock
- The devices have the following two secondary clock sources:
 - ▣ 40 kHz low speed internal RC (LSI RC) which drives the independent watchdog and optionally the RTC used for Auto-wakeup from Stop/Standby mode
 - ▣ 32.768 kHz low speed external crystal (LSE crystal) which optionally drives the real-time clock (RTCCLK)
- Each clock source can be switched on or off independently when it is not used, to optimize power consumption

Clock Tree

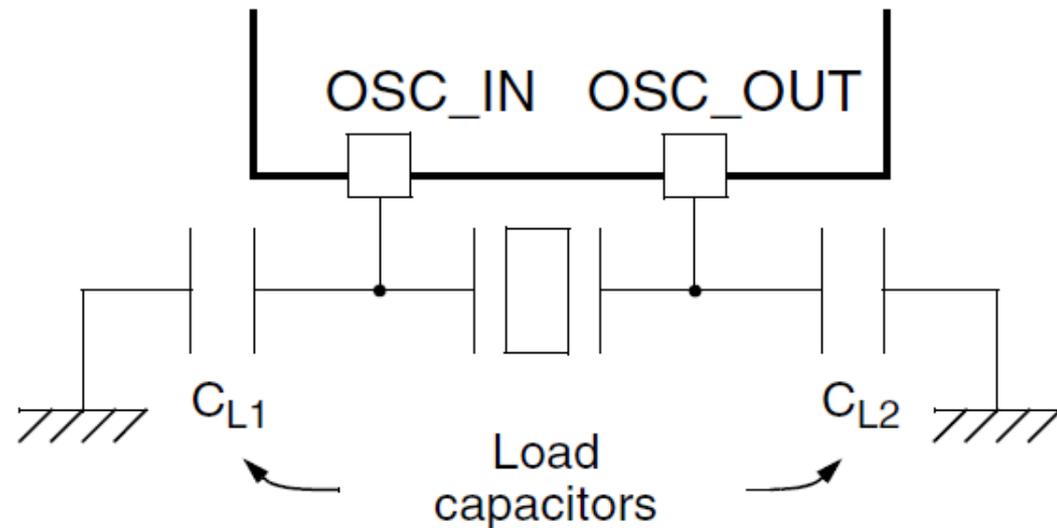


HSE Clock

- The high speed external clock signal (HSE) can be generated from two possible clock sources:
 - ▣ HSE external crystal/ceramic resonator
 - ▣ HSE user external clock



External clock



Crystal/Ceramic resonators

HSI Clock

- The High Speed Internal (HSI) clock signal is generated from an internal 8 MHz RC Oscillator and can be used directly as a system clock or divided by 2 to be used as PLL input
- The HSI RC oscillator has the advantage of providing a clock source at low cost (no external components)
- It also has a faster startup time than the HSE crystal oscillator however, even with calibration the frequency is less accurate than an external crystal oscillator or ceramic resonator
- RC oscillator frequencies can vary from one chip to another due to manufacturing process variations
 - ▣ Each device is factory calibrated by ST for 1% accuracy at $T_A=25^{\circ}\text{C}$.
 - ▣ After reset, the factory calibration value is loaded in the HSICAL[7:0] bits in the Clock control register (RCC_CR)
 - ▣ You can trim the HSI frequency in the application using the HSITRIM[4:0] bits in the Clock control register (RCC_CR)

PLL

- The internal PLL can be used to multiply the HSI RC output or HSE oscillator divided by 16 output clock frequency
- The PLL configuration (selection of HSI oscillator divided by 2 or HSE oscillator for PLL input clock, and multiplication factor) must be done before enabling the PLL
 - ▣ Once the PLL enabled, these parameters cannot be changed
- The PLL output frequency must be in the range of 16-24 MHz

Low Speed Clocks

- The LSE crystal is a 32.768 kHz Low Speed External crystal or ceramic resonator
 - ▣ It has the advantage providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions
- The LSI RC acts as an low-power clock source that can be kept running in Stop and Standby mode for the independent watchdog (IWDG) and Auto-wakeup unit (AWU)
 - ▣ The clock frequency is around 40 kHz.

System Clock (SYSCLK) Selection

- After a system reset, the HSI oscillator is selected as system clock
- When a clock source is used directly or through the PLL as system clock, it is not possible to stop it
- A switch from one clock source to another occurs only if the target clock source is ready (clock stable after startup delay or PLL locked)
 - ▣ If a clock source which is not yet ready is selected, the switch will occur when the clock source will be ready
 - ▣ Status bits in the Clock control register (RCC_CR) indicate which clock(s) is (are) ready and which clock is currently used as system clock

Clock Security System

- Clock Security System can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped.
- If a failure is detected on the HSE clock, the HSE oscillator is automatically disabled, a clock failure event is sent to the break input of the advanced-control timers (TIM1) and an interrupt is generated to inform the software about the failure (Clock Security System Interrupt CSSI), allowing the MCU to perform rescue operations.

RTC and Watchdog Clocks

- The RTCCLK clock source can be either the HSE/128, LSE or LSI clocks. This is selected by programming the RTCSEL[1:0] bits in the *Backup domain control register (RCC_BDCR)*
- This selection cannot be modified without resetting the Backup domain.
- If the Independent watchdog (IWDG) is started by either hardware option or software access, the LSI oscillator is forced ON and cannot be disabled
 - ▣ After the LSI oscillator temporization, the clock is provided to the IWDG

Clock-Out Capability

- The microcontroller clock output (MCO) capability allows the clock to be output onto the external MCO pin.
 - ▣ The configuration registers of the corresponding GPIO port must be programmed in alternate function mode
- One of 4 clock signals can be selected as the MCO clock:
 - ▣ SYSCLK
 - ▣ HSI
 - ▣ HSE
 - ▣ PLL clock divided by 2
- The selection is controlled by the MCO[2:0] bits of the *Clock configuration register (RCC_CFGR)*

Assignments

- ARM Project #2