FPGA Based Backend System for Medical B-Mode Ultrasound Imaging

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Abstract- **Architecture of the backend system of medical B-mode ultrasound machine is introduced. The RF signal after the beam former until the display of the image is handled. Over sampled analog to digital converter (A/D) is used. Signal reconstruction is done by Hilbert Transform Technique that is implemented using finite impulse response filters (FIR) applied on each scan line returning from the beam former. Image reconstruction is done through scan conversion and interpolation modules. The design is applied on Xilinx Spartan3 FPGA. The results are displayed on a CRT monitor.**

Keywords **– Hilbert Transform, Image construction, interpolation , Ultrasound using FPGA .**

I. INTRODUCTION

Medical ultrasound importance in medical diagnosis and health care industry is highly recognized in the recent years. Ultrasound is a diagnostic technique, unlike x-rays, where one does not get exposed to any kind of radiation. the acoustic output of ultrasonic devices can be limited to levels which are known not to be hazardous. this is why ultrasound images are used in imaging many sections of the body (e.g. abdominal, vascular, cardiac ,and obyginacology….).

Recently, portable and lightweight ultrasound scanners have been developed, which greatly expand the range of situations and sites for which medical ultrasound can be used.

Ultrasound systems development is highly influenced by the evolution in digital electronics. The number of functions and image quality increases, and the implementation price for any given function decreases with time. One powerful approach for is to use increasing the flexibility and compactness of an ultrasound scanner is to apply the digital processing techniques on FPGA (Field Programmable Gate Array) digital technology, instead of the traditional microprocessors (MP) and digital signal processors (DSPs) used. This will transform the ultrasound machine from a PC based platform machine to an FPGA based platform machine, that is smaller, cheaper, and with reconfigurable performance.
FPGA means Field Programmable Gate Array. It gives the designer the ability to use the VHDL to program some configurable Logic Blocks to build the system he needs. Also it gives the ability to reconfigure the design and so reprogram it again. The FPGA is used to perform some DSP functions giving appropriate performance, high speed with low cost and in a small size.

This shall decrease the cost of the ultrasound machine, and as a consequence the cost of the patient diagnostic session will decrease, and health care level will improve specially in rural areas.

II. SYSTEM ARCHETICTURE

A block diagram illustrating the data flow in our proposed system is shown in Fig(1).

First of all we have to note that our system is not a complete instrument, we are only making the part after the beam forming unit, so here we assume that we already got the signal after the summation in the beam forming, so our goal is the signal processing stage after the beam forming. We start with the A/D, then the signal envelope detection, where the first step of image signal reconstruction is made and the main information of the original signal are deduced, after that the envelope of each scan line resulted is passed to the scan conversion where we convert each point in each scan line from the polar coordinates to Cartesian coordinates to fit right on the screen then and right before display, we insert the signal to an interpolation filter that interpolate the scan lines points to fill the black empty dots in the image, and finally the image is stored in a SRAM buffer from which it is handed to the display driver so that the image is directly displayed on the VGA monitor. Also there is an upgrade to make a user interface which provides options to control the output from this module, options such as freeze and unfreeze the image on the screen. Other future modifications can be providing the system with a USB computer interface, which gives the user the option of connecting this module to a workstation or another FPGA system that provides means for image processing and advanced user interface.

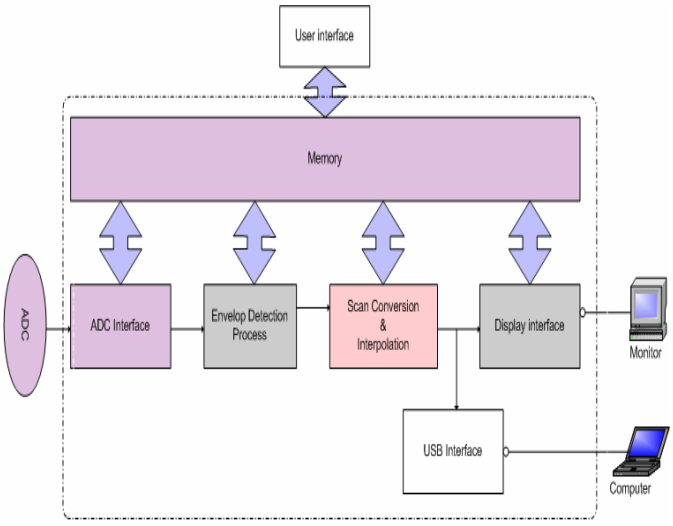

Fig. 1. Block diagram of ultrasound backend system.

The previous block diagram shows our proposed system that represent the unit in ultrasound system that handle the echo signals after being summated. It consists of six main blocks represented in the next paragraphs.

A. Analog to digital conversion(A/D):

The summated signal came from the beam former enter on an analog to digital converter ths1301 that digitize the signal up to 25 MHZ . Then it stores it in FPGA memory to e handled after that by the Hilbert transform filters. As for first trials we used the 0808 ADC to test the ability to interface to FPGA then we went through using the thes1301 to have more frequencies range. The clock of ADC was generated from the FPGA through its Digital clock manager where we divided the source clock from oscillator on the kit 50 MHZ by 2 so that we have 25 MHZ that needed for that ADC.

B. Memory Interface:

After having the data, we need to store it in memory to apply the next stages on it. In our starter kit we had 3 types of memory. First was the external SRAM that can store = one Mbyte. Second inside the FPGA , where there is distributed Block of RAM. Also you may use the LUT in the CLB in FPGA to implement extra memory capabilities.

C. Envelop detection part:

Usually envelope detection requires that we get the I & Q components of the RF signal, so that to get the over all magnitude. The I component represent the in phase component, and the Q phase represents the quadrature component of the signal (90 phase shift). There are certain techniques used to get the I & Q components, especially for ultrasound signal.
Conventional approaches to generating I/Q data include analog/digital base band demodulation, and use of the Hilbert transform. Using a demodulation based approach to generate I/Q data would necessitate significant extra circuitry on each channel, and use of the Hilbert transform would require a significant amount of memory to hold the raw RF data. Digital memory is generally inexpensive and dense, That is why we choose to use the Hilbert transform approach, especially that we are using FPGA, where we already have memory, and we target low cost, small size machine.

D. Image reconstruction:

In standard mechanically-scanned B-Mode, Pulse-echo ultrasonic imaging data are usually obtained in polar form .for each of several different angles of the transducer, the echo is digitized at a fixed sampling frequency. Scan conversion is the process of converting the acquired and processed polar coordinate ultrasound data into the Cartesian raster data used by standard display monitors. This is traditionally the stage at which interpolation between envelope-detected signal lines occurs, to determine the echo amplitude values that must be written to a display memory whose read-out is in rectangular co-ordinates, even though the echo lines may have been collected in a polar (or other) co-ordinate system ,so to reconstruct an image we made two process scan conversion and interpolation.

SCAN CONVERSION: Once data processing is complete, scan conversion is performed. Scan conversion converts the collected ultrasound data (which is in polar coordinates) into Cartesian coordinates. WE tried here by using Matlab make m-files or by using Xilinx Blocks in the Matlab library, but we did the first method we used m-files to make a scan conversion code and we used to equations to convert from the polar coordinates to Cartesian and also by using real data from transducer and here is the two equations that we used to do that
X=r cos (theta),
Y=r sin (theta).
See fig.2.

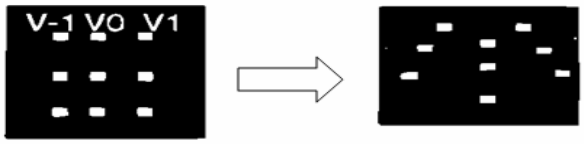

Fig. 2. Shows the scan conversion effect on data.

Where the data we used has been taken from a transducer with:
-Radius of probe = 60 mm
-Linear step of probe = 0.9 mm (you can compute the angular step as 0.9/60(
-Number of lines = 80
-Depth of penetration = 16 cm
The scanned object in the resulted image was a standard ultrasound quality assurance phantom in the IBE Company for medical ultrasound equipments.

E. Display part:

The VGA driver is the core of this task of project, it's a VHDL module we implemented to provide the main 5 signals t are needed by the VGA port to drive the monitor. This module also contains the part that provides the gray scale control, which until now reached only 4 levels.
So, this module is divided to 2 parts:

- VGA timing module: that provides the HS & VS signals.
- Mapper & PWM module: which provide the corresponding RGB values for one of 4 Gray scales.

We could have the lines displayed on the PC monitor and and we could control colours till 8 colours only and we are working on having much Gray levels and interfacing it to memory to display our stored image.

III. RESULTS

The total system as shown in the system architecture was not integrated together but each part was simulated by

Xilinx and matlab tools to assure that it produces the desired output. For ADC part codes it was simulated by ModelSim program that Xilinx provide to simulate the total system cycle virtually.

And for Image construction part , it was simulated by Matlab where fig.4 where produced while fig.3 representing the original received summated signal from the ultrasound probe as we mentioned its details in the Image Reconstruction in System Architecture.

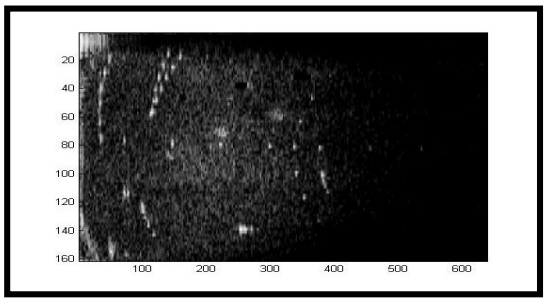

Fig. 3. Shows the original received image.

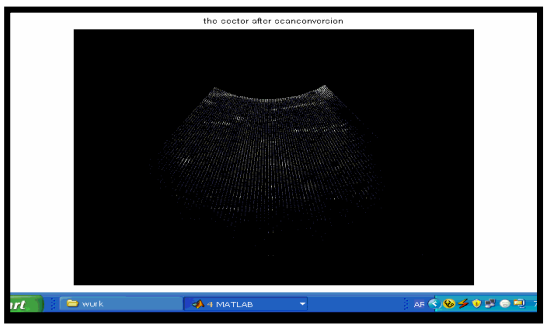

Fig. 4. Shows the resulted Image.

IV. Discussion

The resulted image was having some missing lines due to not applying the Interpolation algorithms onto the image. This was because when we applied the interpolation algorithms, it produced blurred and unclear images. We still are working to enhance that. Also some hardware problems we faced in the interfacing the ADC circuit we will explain and solve it in next papers.

IV. Conclusion

Our project was to build the system that can handle the signal after summation stage till display. We cannot say that it totally works but we can say that tasks separately work alone. The phase of integration needs more time to integrate each with others and see results but we will try to do that through next days.

This project has taught us a lot about the new technology FPGA that we did not use before and how to deal with it beside implementing important functions using it. On the other hand it gave us a very good overview on the ultrasound processing techniques and defects of ultrasound systems that need enhancement. Also it involves us into the market needs and how to satisfy.

Concluding what system can perform:

- We can reconstruct any image from stored matrix in a convex shape
- We can interface ADC to kit and drive its circuit
- We can display images through VGA port of the kit
- We can build filters that deal with signals
- We can place any code on our kit and stimulate it
- We can use the power supplies provided by the kit to drive other circuits
- We can generate any clock from kit to drive other hardware circuit

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