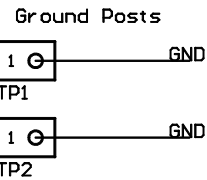
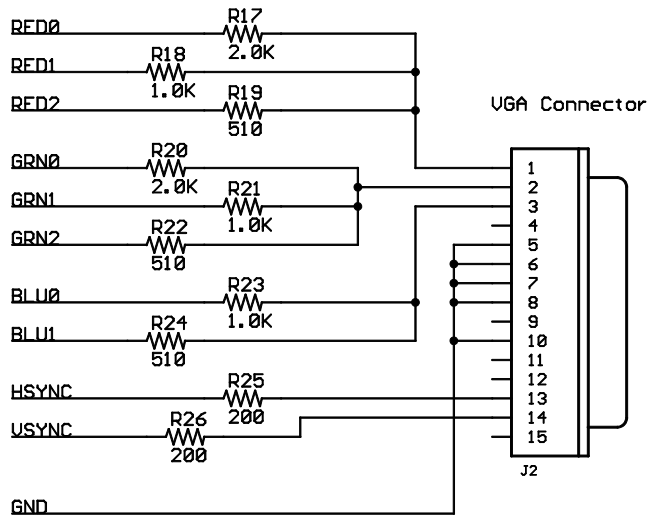
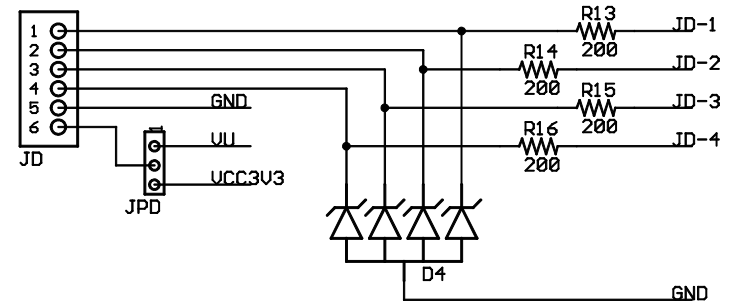
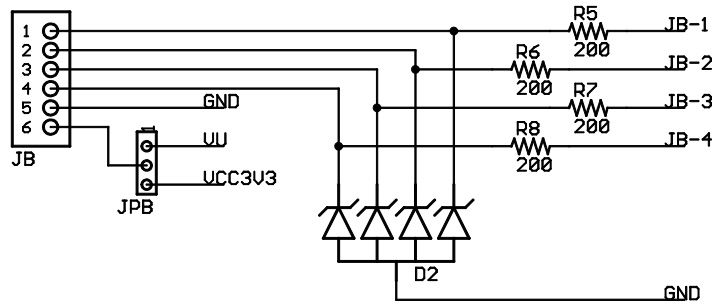
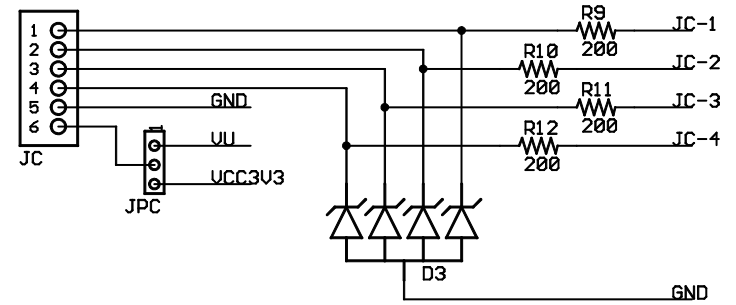
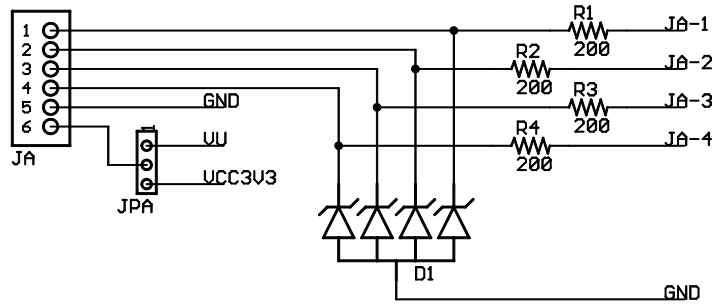
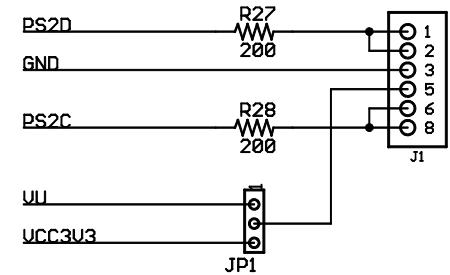


PMOD Interface Connectors



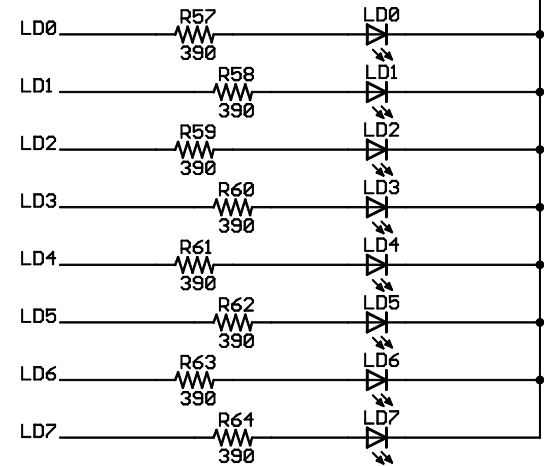
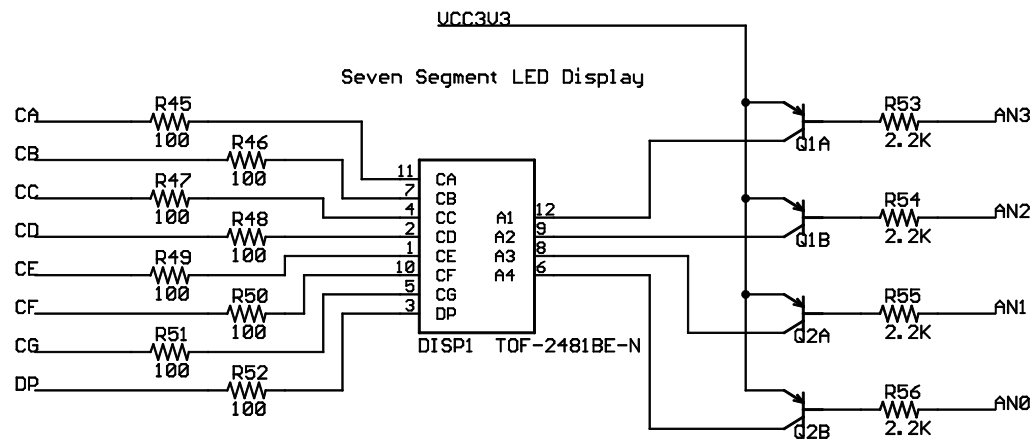
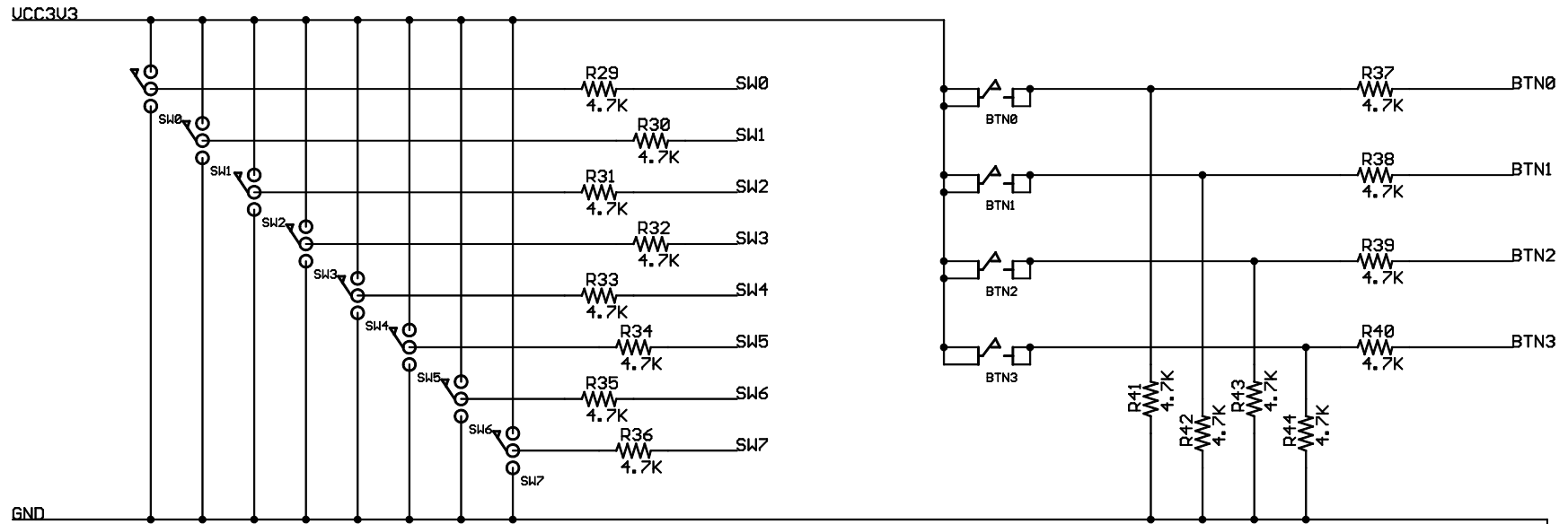
PS/2 Keyboard Connector



WEEE

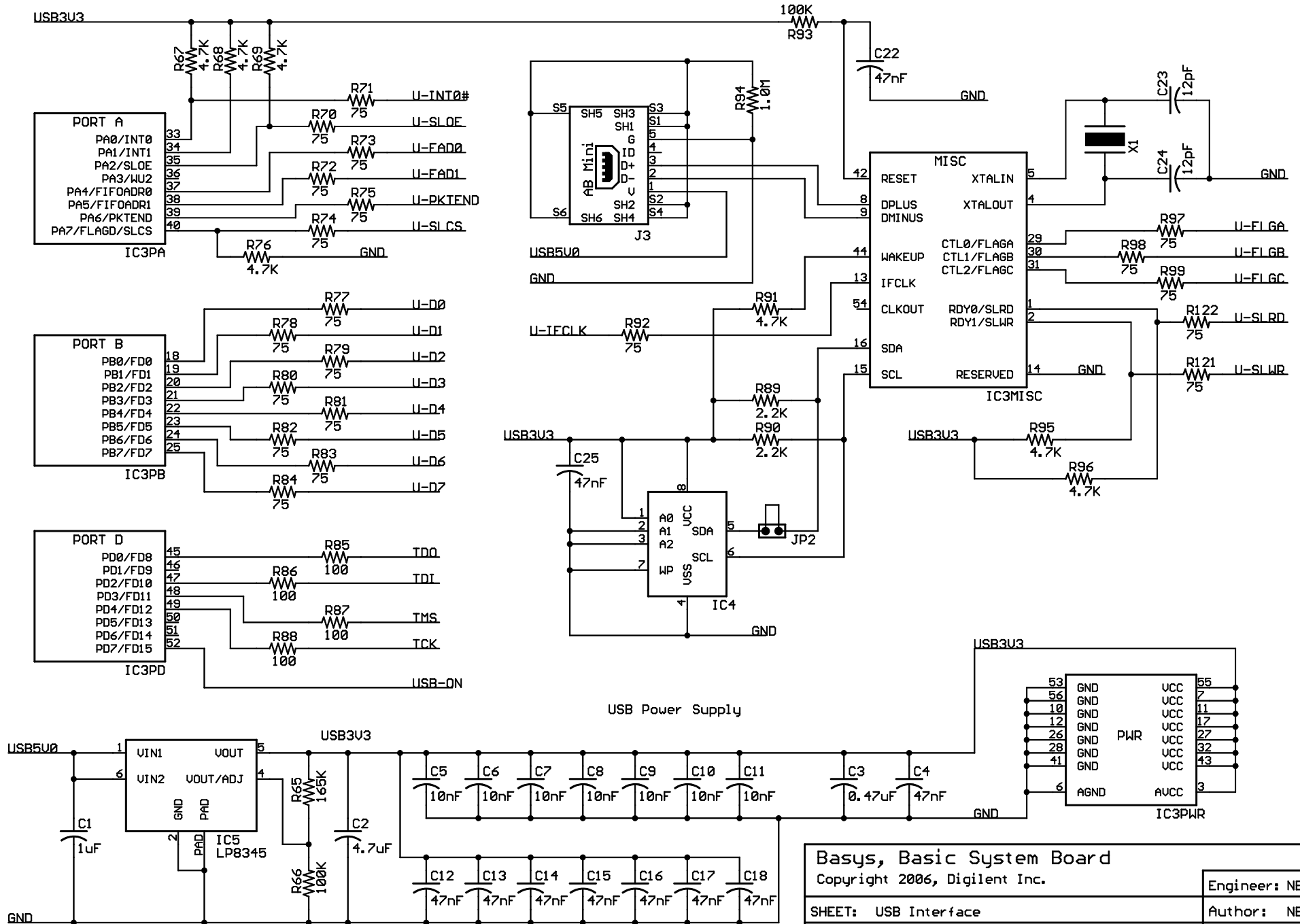
Basys, Basic System Board Copyright 2006, Digilent Inc.		Engineer: NEA
SHEET: I/O Connectors		Author: NEA
TITLE: Basys		Rev: E
Basys	Doc#: 500-107	Date: 10/24/2006
		Sheet: 1/8

On-Board I/O Devices



Basys, Basic System Board		Engineer: NEA
Copyright 2006, Digilent Inc.		Author: NEA
SHEET: On-Board I/O		Rev: E
TITLE: Basys		Sheet: 2/8
Doc#: 500-107	Date: 10/24/2006	

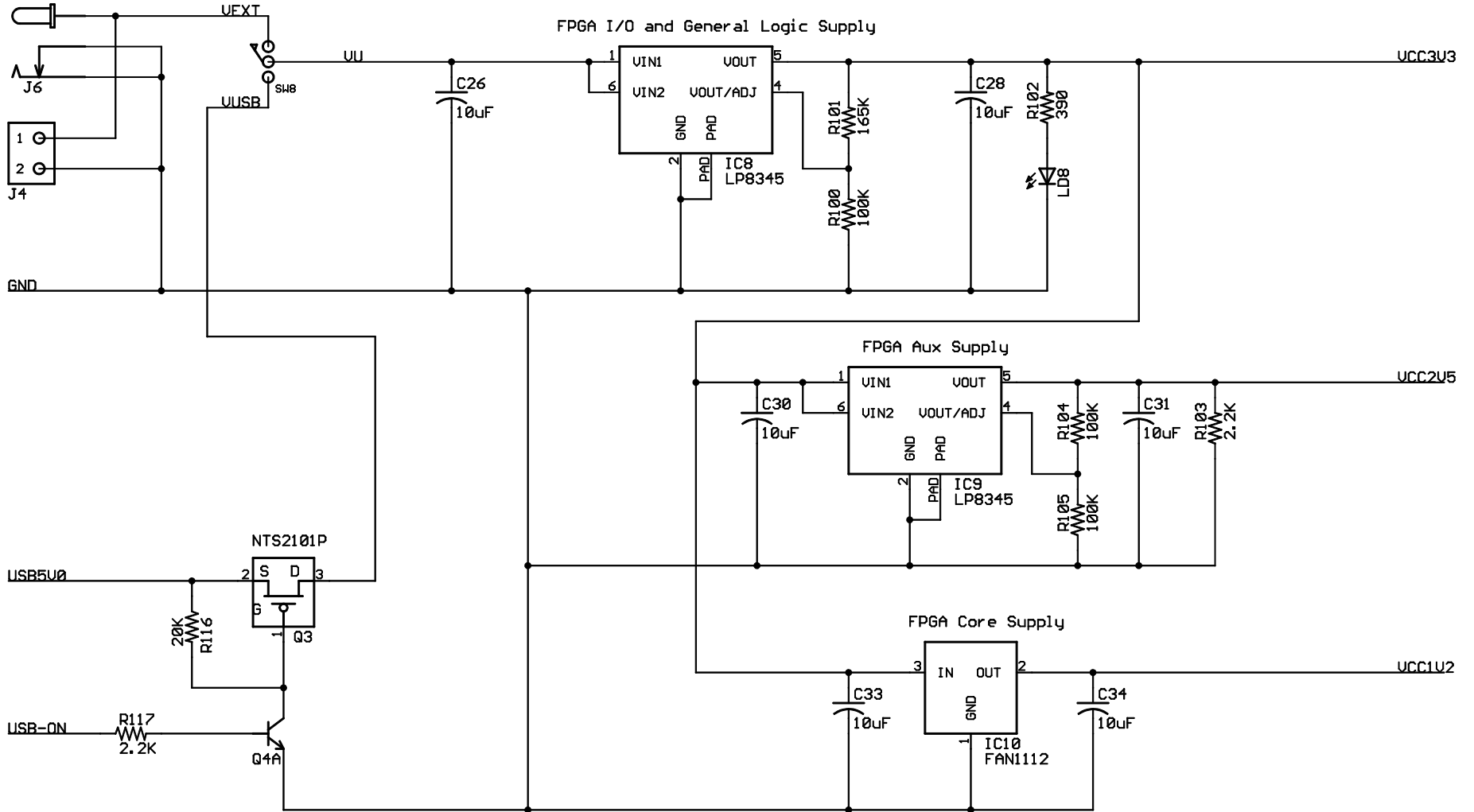
USB Interface



Basys, Basic System Board		Engineer: NEA
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SHEET: USB Interface		Rev: E
TITLE: Basys		Doc#: 500-107
Date: 10/24/2006		Sheet: 3/8

# Main Board Power Supplies

Uext 3.6 - 9U



Basys, Basic System Board

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Engineer: NEA

SHEET: Power Supply

Author: NEA

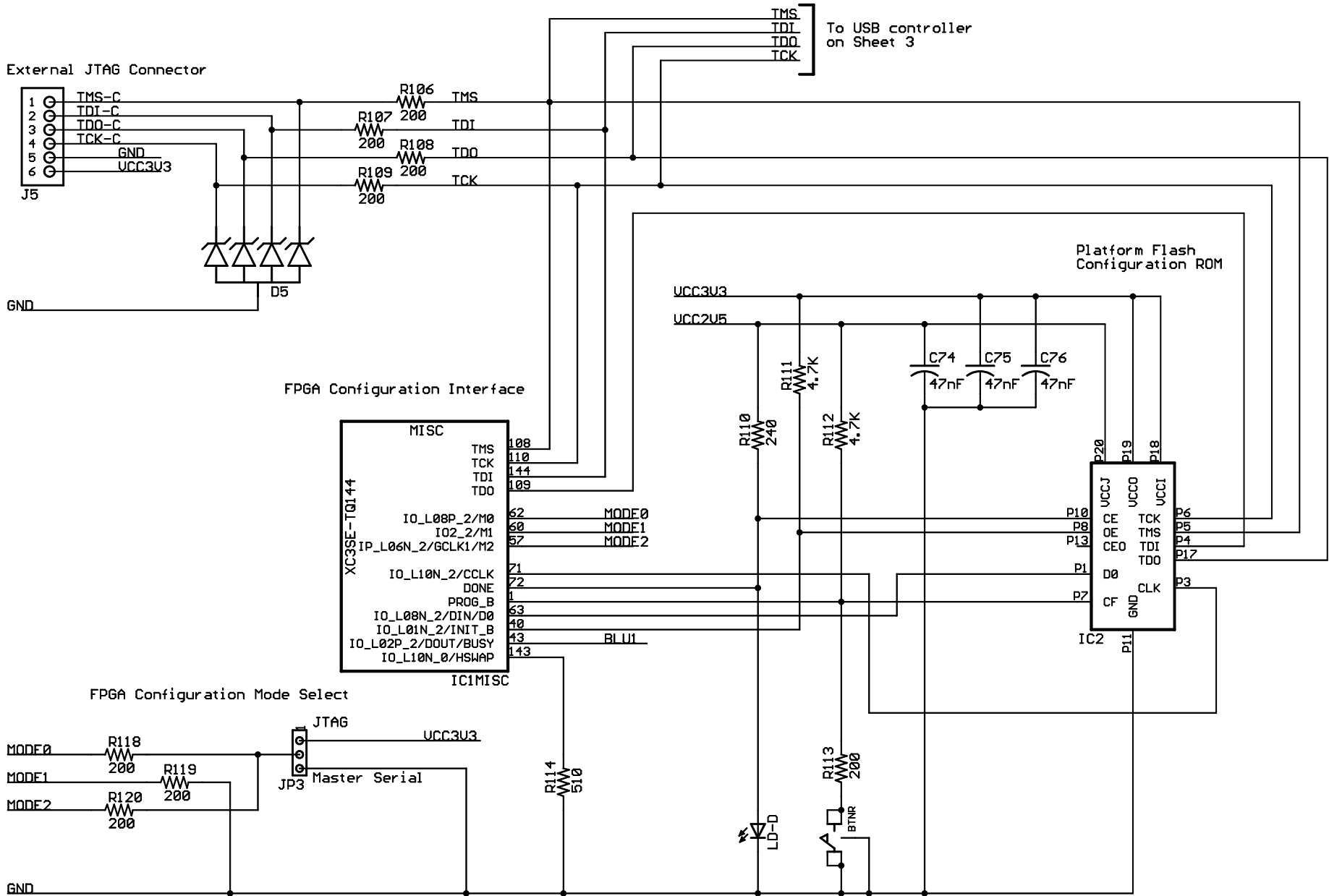
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Rev: E

Doc#: 500-107

Date: 10/24/2006

Sheet: 4/8



To USB controller  
on Sheet 3

External JTAG Connector

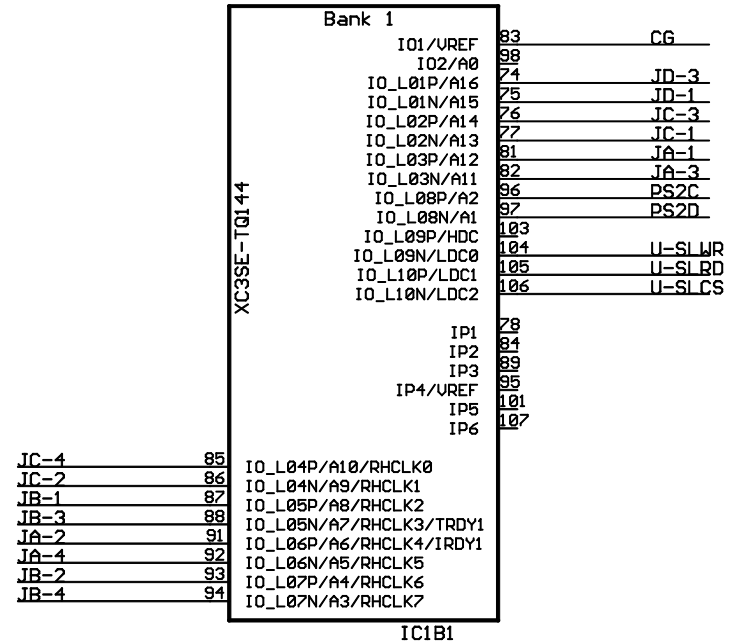
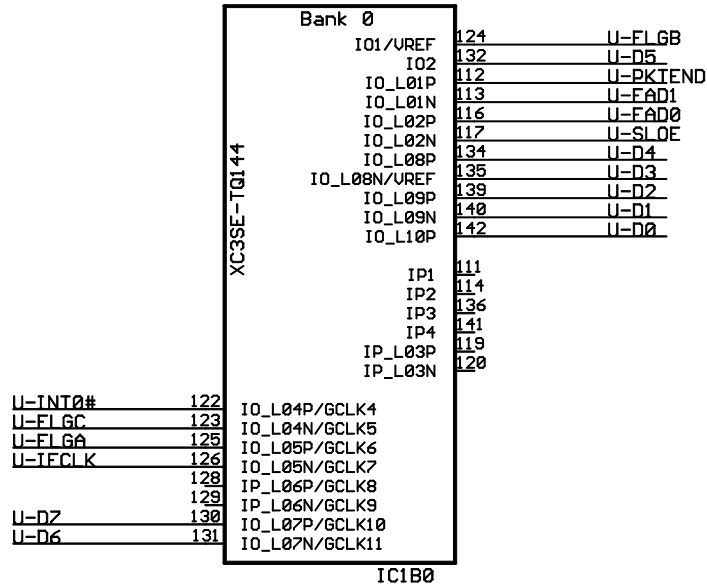
FPGA Configuration Interface

Platform Flash  
Configuration ROM

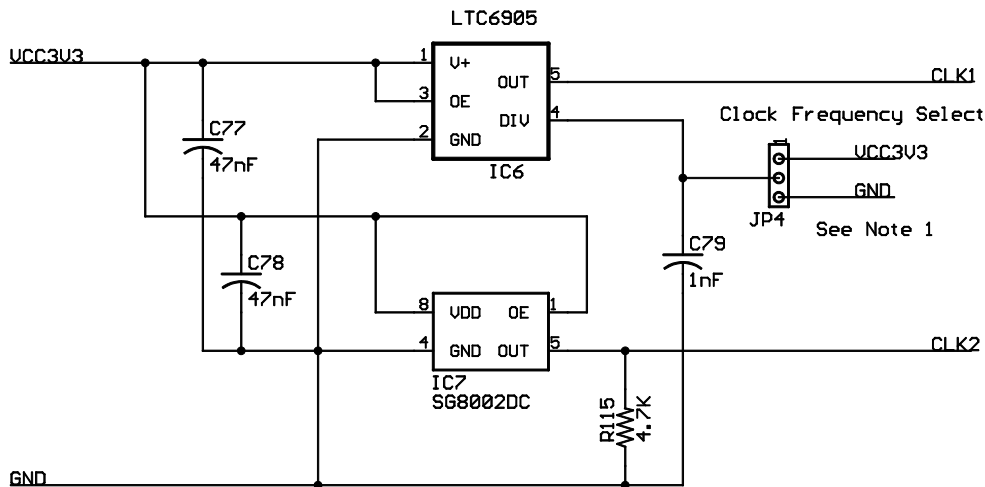
FPGA Configuration Mode Select

Basys, Basic System Board		Engineer: NEA	
Copyright 2006, Digilent Inc.		Author: NEA	
SHEET: FPGA Configuration		Rev: E	
TITLE: Basys		Date: 10/24/2006	
Doc#: 500-107	Date: 10/24/2006	Sheet: 5/8	

FPGA I/O Banks



Clock Oscillators



Note 1: Use shorting block in UCC3V3 position for 100 Mhz  
 Use no shorting block for 50Mhz  
 Use shorting block in GND position for 25Mhz

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SHEET: FPGA I/O Banks

Author: NEA

TITLE: Basys

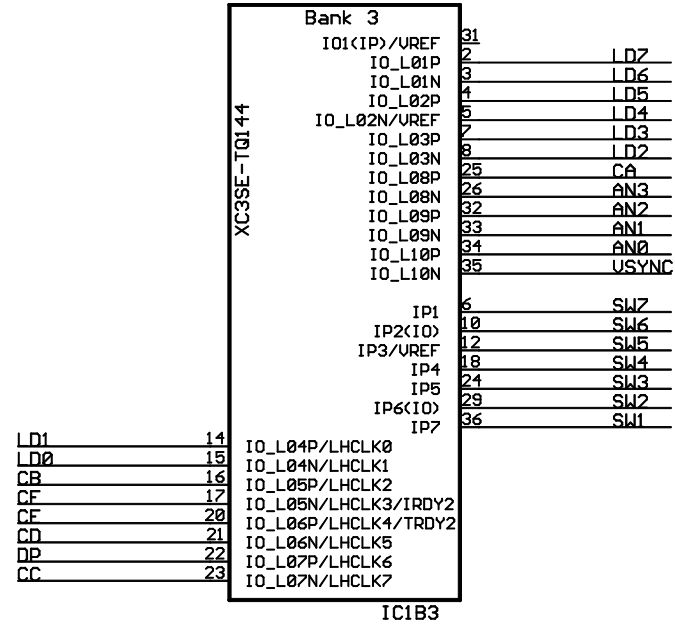
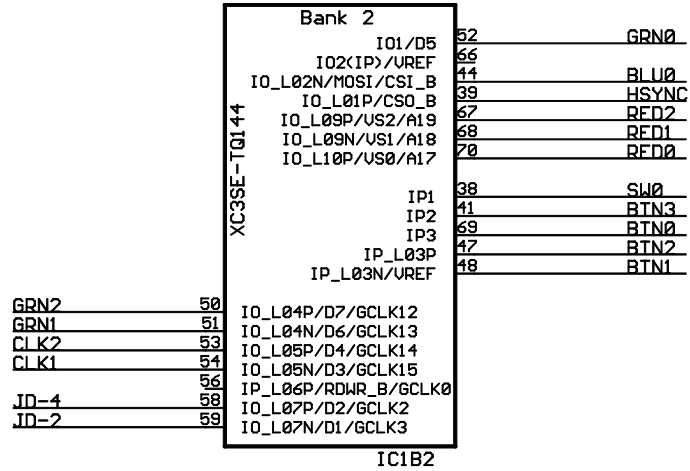
Rev: E

Doc#: 500-107

Date: 10/24/2006

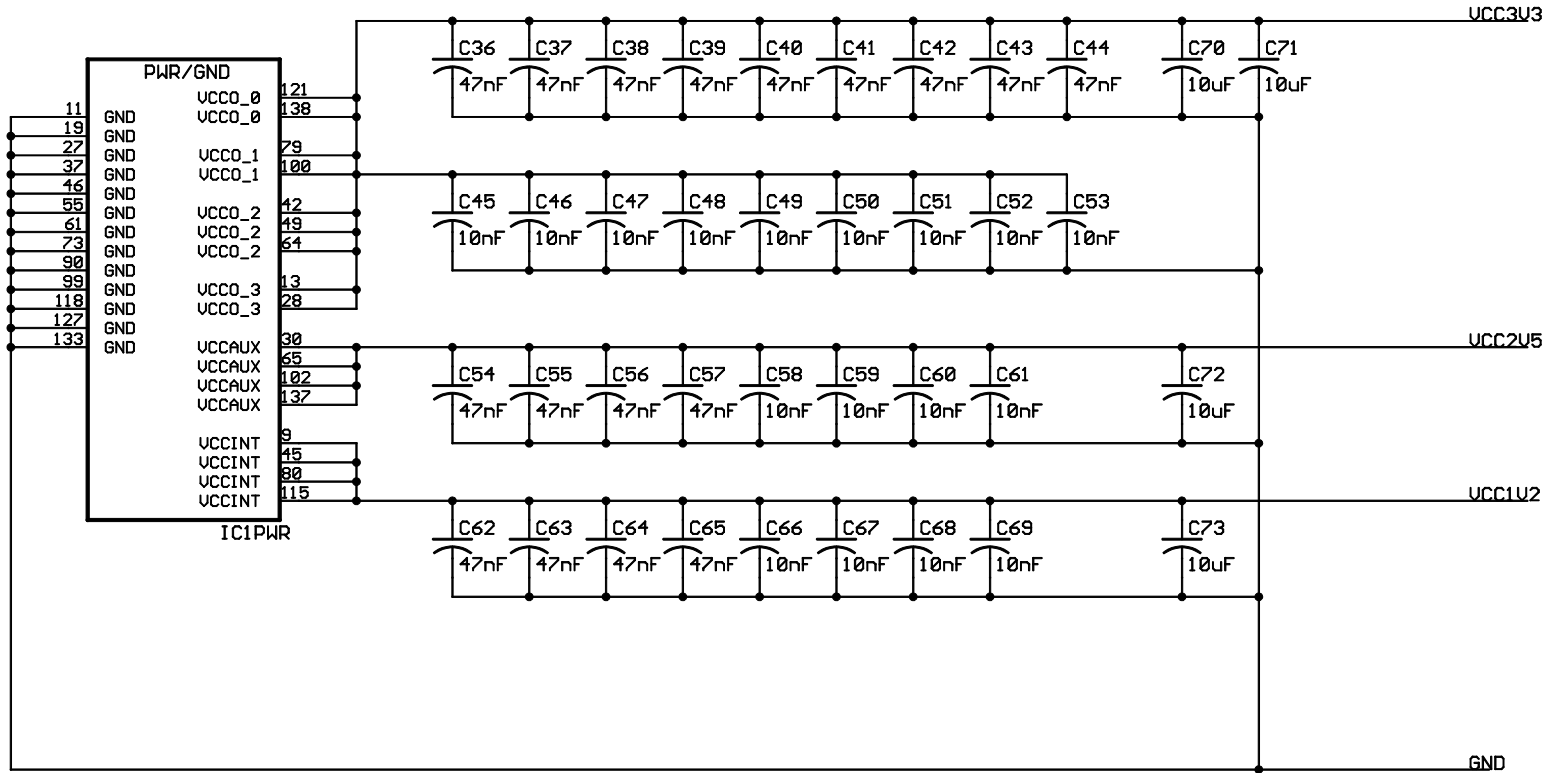
Sheet: 6/8

FPGA I/O Banks



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SHEET: FPGA I/O Banks		Rev: E
TITLE: Basys		Sheet: 7/8
Doc#: 500-107	Date: 10/24/2006	

### FPGA Power Supply Bypassing



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SHEET: FPGA Power Supply Decoupling

Author: NEA

TITLE: Basys

Rev: E

Doc#: 500-107

Date: 10/24/2006

Sheet: 8/8