Cairo University *Time Allowed: 1 Hour*
Biomedical Engineering Department *Open-Book/Open-Notes*

Medical Electronics IV Mid-Term Exam (Part II) – May 2009

Student Name:	**Sec.:**	**B.N.:**

Solve as Much as You Can – Maximum Grade: 100 Points

Q1. Answer the following questions by marking the best answer among the choices given (3 points each):

1. Concurrent processing in FPGA is assumed for all models except … model.
   a. Structural
   b. Behavioral
   c. Sequential (*)

2. To allow engineers to focus on high-level design considerations, … model is prefered.
   a. Structural
   b. Behavioral (*)
   c. Schematic

3. Bus implementation of a given 1-bit multiplexer design can be obtained using …
   a. Vector inputs/outputs (*)
   b. Bus slice design
   c. Conditional bus assignment

4. To verify a given VHDL design, … is performed prior to actual implementation.
   a. Simulation (*)
   b. Synthesis
   c. Structural realization

5. In a typical design cycle, simulation is done …
   a. Once
   b. Twice (*)
   c. Three times

Q2. Mark the following statement as either True (T) or False (F) (1 point each):

1. VHDL can be used to describe any electronic circuit. (F)
2. Schematic editor is a way to enter VHDL directly into Xilinx ISE. (F)
3. It is possible to simulate 2-lead ECG signals from a C8051F020 microcontroller. (T)
4. Microcontroller DAC must utilize at least one timer to operate. (F)
5. It is possible to program the hysteresis behavior of the C8051F020 comparators (T)

Q3. [35 Points] Given signal sources **a**, **b**, and **c**; selection lines **s0** and **s1**; and a desired output **out**:
a) write a VHDL code to implement the following truth table using behavioral model
b) write a VHDL code to implement the following truth table using sequential model
c) List the changes that must be made to parts (a) or (b) to accept 8-bit bus signals **a**, **b**, and **c** and a desired 8-bit output **out**

s0	s1	out
0	0	a OR b OR c
0	1	a AND b AND c
1	ϕ	0

(Q3-a) Behavioral Model Answer:

```
ENTITY Q3 IS
PORT ( a, b, c : IN std_logic;
       s0, s1 : IN std_logic;
       out : OUT std_logic);
END mux;

ARCHITECTURE behavioral OF mux IS
SIGNAL select : INTEGER;
BEGIN
out<=a or b or c WHEN s0='0' AND s1='0' ELSE
    a and b and c WHEN s0='0' AND s1='1' ELSE
    0;
END behavioral;
```

(Q3-b) Sequential Model Answer:

```
ENTITY Q3 IS
PORT ( a, b, c : IN std_logic;
       s0, s1 : IN std_logic;
       out, : OUT std_logic);
END mux;

ARCHITECTURE sequential OF mux IS
PROCESS (a, b, c, s0, s1 )
BEGIN
IF s0 = '0' and s1 = '0' THEN
  out := a or b or c;
ELSEIF s0 = '0' and s1 = '1' THEN
  out := a and b and c;
ELSE
  out := 0;
END IF;
END PROCESS
END sequential
```

(Q3-c) change entity part as

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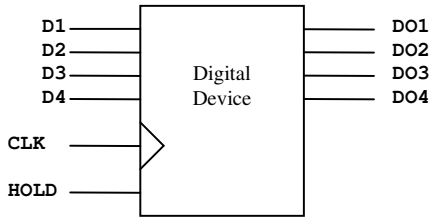
```
ENTITY Q3 IS
PORT (a,b,c: IN std_logic_vector(7 downto 0);
       s0, s1 : IN std_logic;
       out: OUT std_logic_vector(7 downto 0)
      );
END mux;
```

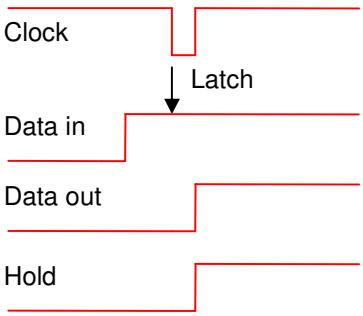
Q4. [35 Points] Write a VHDL code to implement a digital device with the following specifications:



a) 6 inputs representing data lines **D1**, **D2**, **D3**, and **D4**, data hold **HOLD** and clock **CLK**.
b) 4 outputs **DO1**, **DO2**, **DO3** and **DO4 .**
c) When **HOLD** = 0, the outputs **DO1**, **DO2**, **DO3**, and **DO4** take the values of their respective inputs **D1**, **D2**, **D3** and **D4** with a trailing edge transition of the clock **CLK** (that is, when the clock **CLK** changes from 1 to 0, **DO1=D1**, **DO2=D2**, **DO3=D3**, and **DO4=D4**)
d) When **HOLD** =1, outputs **DO1**, **DO2**, **DO3**, and **DO4** do not change with any transition of the clock **CLK**.

Q4 Answer:

The clock that works with a trailing edge transition looks like this :



Model Answer (non-exclusive, your answer may still be correct)

```
entity Q4 is
    port (Di:     in  STD_LOGIC_VECTOR(3 downto 0);
          CLK,HOLD:     in STD_LOGIC;
          Do:     inout  STD_LOGIC_VECTOR(3 downto 0));
end Q4;

architecture behavioral of Q4 is
begin
Do <= Di when (HOLD='0' and CLK=0) else
      Do;
            -- CLK =0 means a change from 1 to 0
            -- CLK =0 means a change from 1 to 0
end behavioral;
```

Q5. [30 Points] Consider a microcontroller-operated heater shown below.
Part (a) Design a C8051F020 project that would enable the linear control of the heater to adjust the temperature to a predefined value T_d. The desired control is such that the heater is linearly controlled through a transistor operating in the linear region using an analog control signal from a microcontroller. The control signal is generated depending on the feedback from a temperature sensor measured by an external 8-bit ADC connected to P1 of the microcontroller. Assuming the measured temperature value to be Tm, the control signal output has the form:

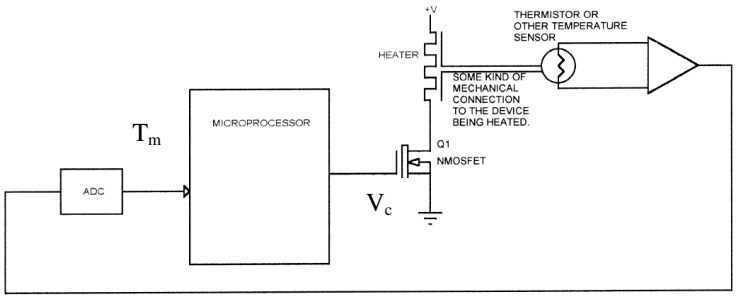
$$V_c = 2(T_m - T_d) \quad \text{if } T_m > T_d$$
$$0 \quad \text{otherwise}$$

Assume that the ADC used is of 8-bit FLASH type (i.e., requires no clock and its digital reading corresponds to the temperature value whenever it is read).

Part (b): if the control signal is changed to take the form:

$$V_c = 2(T_m - T_d)$$

regardless of the values of T_m and T_d, would it still be possible to implement this controller using C8051F020? Provide the reasons for your answer. (Hint: answer is Yes or No with a brief justification – no code necessary for this part)



Q5 (a):

Just like lab 9 but you will basically feed the DAC the data calculated from Vc equation. The data read from port 1 of the microcontroller will correspond to Tm while Td should be a constant value in the program. If the result of the calculation is below 0, the output Vc =0, otherwise, the value is calculated and sent to the DAC register.

Q5 (b):

NO: since the DAC cannot output negative values.