Cairo University *Time Allowed:1½ Hours*
Biomedical Engineering Department *Open-Book/Open-Notes*

Medical Electronics IV Term Exam (Part II) – June 2009

Solve as Much as You Can – Maximum Grade: 37.5 Points

Q1. Answer the following questions by marking the best answer among the choices given (1.5 points each):

1. Concurrent processing in FPGA is assumed for … model.
    a. Simulation
    b. Behavioral (*)
    c. Sequential

2. To allow engineers to have more control on their design implementation, … model is prefered.
    a. Structural (*)
    b. Behavioral
    c. Schematic

3. Bus implementation of a given 8-bit adder design can be efficiently designed using …
    a. Vector inputs/outputs
    b. Bus slice design (*)
    c. Conditional bus assignment

4. To implement a given VHDL design, … must be performed.
    a. Simulation
    b. Synthesis (*)
    c. Structural realization

5. During synthesis, designer cannot impose design constraints on …
    a. Power consumption
    b. behavioral model (*)
    c. Operating speed

6. Cause-and-effect relationships in VHDL code are a function of …
    a. Where a statement occurs in the VHDL code
    b. How time is modeled (*)
    c. Post-synthesis simulation results

Q2. Mark the following statement as either True (T) or False (F) (1 point each):

1. VHDL can be used to describe any digital electronic circuit. (T)
2. Schematic editor is the only way to enter VHDL directly into Xilinx ISE. (F)
3. Selected signal assignment code can be easily converted to conditional assignment code. (T)
4. An 8-bit multiplier implemented using bit-slice design need minimal effort to be extended to 16-bit multiplier. (T)
5. A synthesizer produces low-level structural description of a circuit based on its VHDL description (T).
6. A behavioral circuit design is essentially a plan of how a digital circuit is to be constructed (F)
7. it is far easier and less time consuming to define a given circuit using structural methods (F)
8. Designers should focus on behavioral design and need not understand the synthesis process very well. (F)

Q3. [10 Points] Given signal sources **a**, **b**, **c** and **d**; selection lines **s0** and **s1**; and a desired output **out**:
a) write a VHDL code to implement the following truth table
b) List the changes that must be made to parts (a) to accept 8-bit bus signals **a**, **b**, **c** and **d** and a desired 8-bit output **out**

s0	s1	out
0	0	(a OR b) AND (c OR d)
0	1	(a AND b) OR (c AND d)
1	ϕ	0

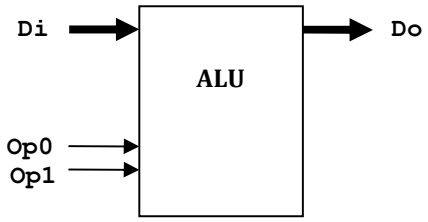
(Q3-a)

Similar to midterm problem Q3

(Q3-b)

Similar to midterm problem Q3

Q4. [10 Points] Write a VHDL code to implement an Arithmetic and Logic Unit (ALU) on an FPGA with one 8-bit input **Di** and 2-bit op code **Op0** and **Op1** and one 8-bit output **Do**. The ALU works as shown in table.



Op1	Op0	Output Do
0	0	RR Di
0	1	RL Di
1	0	CLR Di
1	1	SWAP Di

Hint: Recall that,
RR: The 8 bits in **Di** are rotated one bit to the right. Bit 0 is rotated into the bit 7 position
RL: The 8 bits in **Di** are rotated one bit to the left. Bit 7 is rotated into the bit 0 position
CLR: Clears the output to zeros
SWAP: interchanges low order 4-bit nibbles **Di**[3-0] with high order 4-bit nibbles **Di**[7-4]

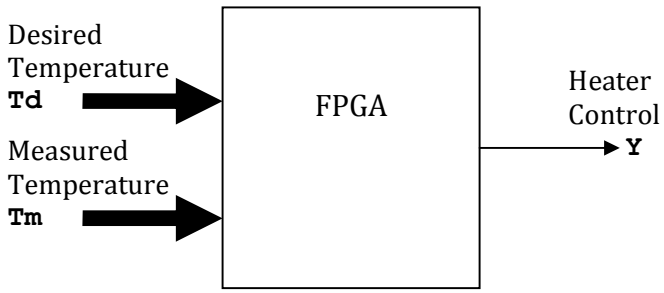
Q4 Answer:

Similar to Shifter example in lectures in first 2 operations, 0 output for third operation, Di(3 downto 0)&Di(7 downto 4) for the last operation

Q5. [10 Points] Consider an FPGA-operated incubator heater shown below. It is required to design an FPGA project that would enable the ON/OFF control of the heater to adjust the temperature to a predefined value Td. The desired control is such that the desired (**`Td`**) and measured (**`Tm`**) temperatures are converted into digital data and fed into the FPGA module. The FPGA outputs a control signal **`Y`** to control the heater such that the heater is turned on (**`Y=1`**) when the measured temperature is lower than the desired, and turned off (**`Y=0`**) otherwise.

a) Provide the VHDL code of the FPGA project described above when **`Td`** and **`Tm`** are 1-bit each.

b) Provide the VHDL code of the FPGA project described above when **`Td`** and **`Tm`** are 4-bits each.



Q5 (a):

Similar to comparator example with only GT (greater than) output

Q5 (b):