



Lecture 8

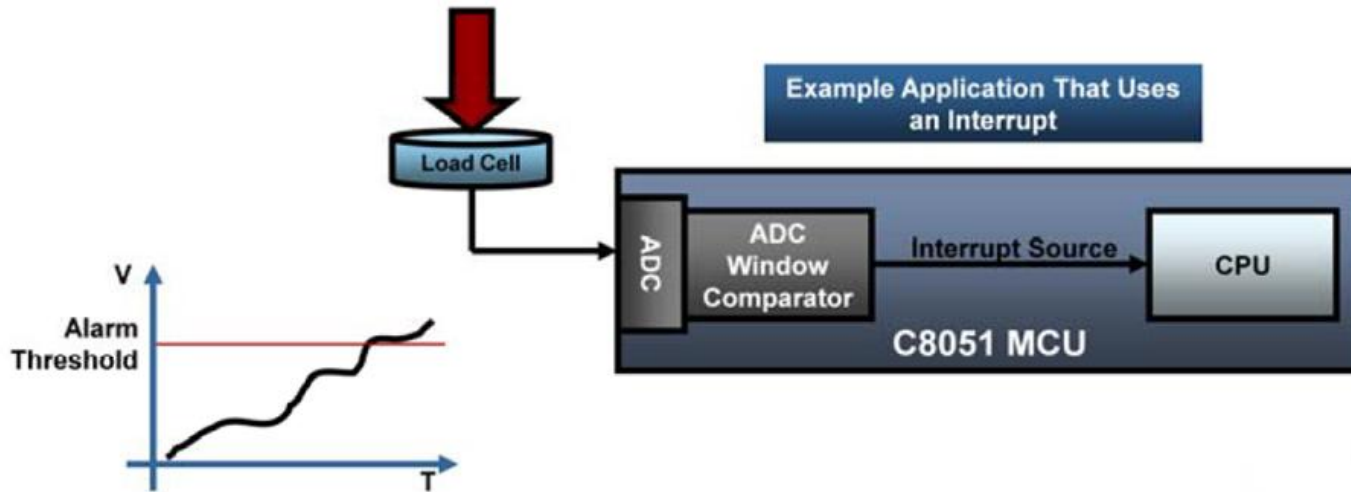
Interrupts

Interrupts

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Introduction

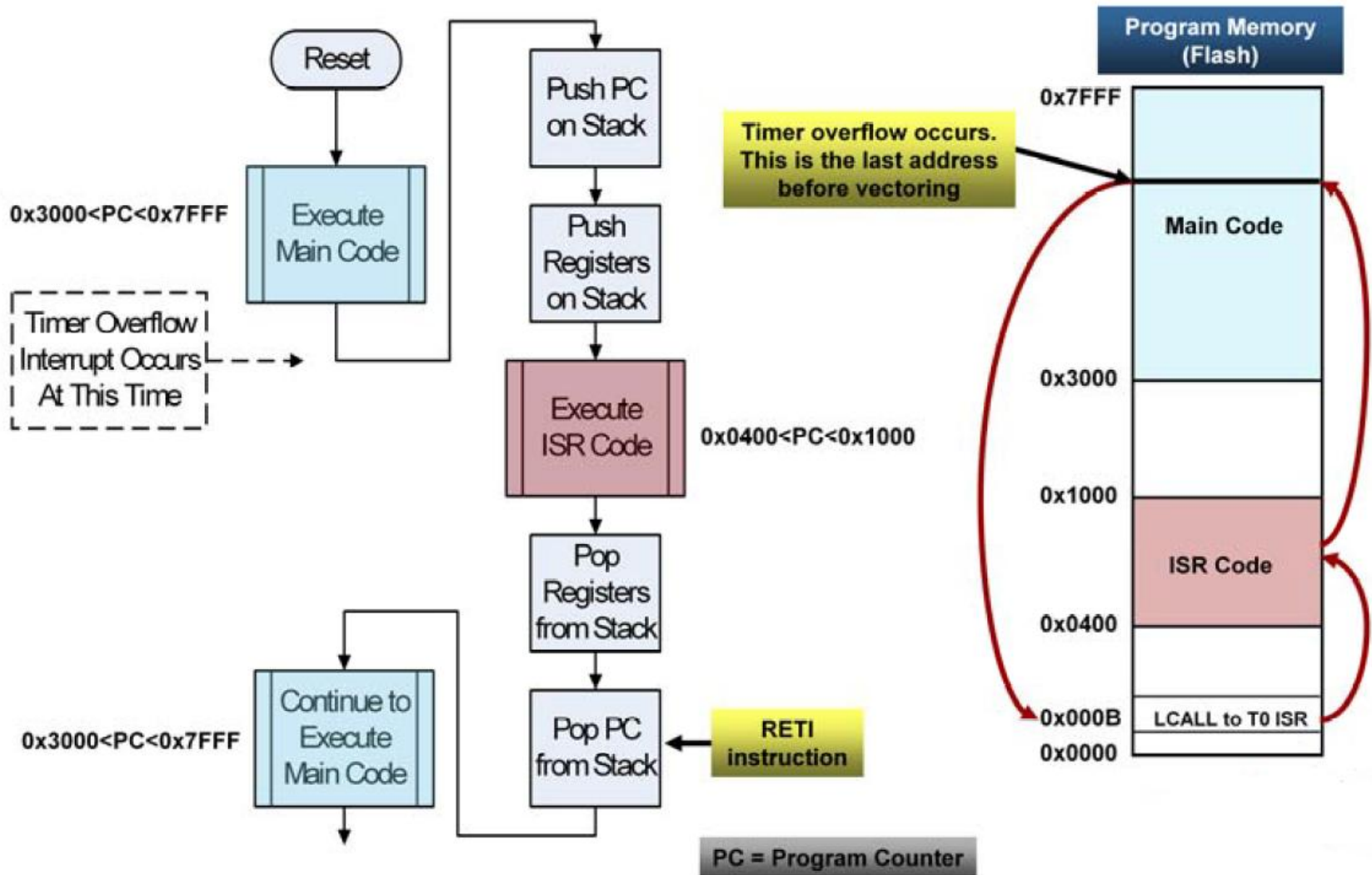
- ◆ An interrupt is the occurrence of a condition that causes a temporary suspension of a program while the condition is serviced by another (sub) program
- ◆ Interrupts are important because they allow a system to respond asynchronously to an event and deal with the event while in the middle of performing another task
- ◆ An **interrupt driven system** gives the *illusion* of doing many things simultaneously
- ◆ The (sub) program that deals with an interrupt is called an **interrupt service routine (ISR)** or **interrupt handler**



Introduction

- ◆ The ISR executes in response to the interrupt and generally performs an input or output operation to a device
- ◆ When an interrupt occurs, the main program temporarily suspends execution and branches to the ISR
- ◆ The ISR executes, performs the desired operation, and terminates with a “return from interrupt” (RETI) instruction
 - The RETI instruction is different from the normal “RET” instruction

Execution Flow



Interrupt Organization

- ◆ The C8051F020 supports 22 interrupt sources, including:
 - 4 external interrupts (/INT0, /INT1, Interrupt 6 and Interrupt 7)
 - 5 timer interrupts (Timer 0 through 4 Overflow)
 - 2 serial port interrupts (UART0, UART1)
- ◆ Each interrupt source has one or more associated **interrupt-pending** flag(s) located in an SFR
- ◆ When a peripheral or external source meets a valid interrupt condition, the associated interrupt-pending flag is set to 1
 - These interrupt flags are “level sensitive” in that if the flag is not cleared in the ISR by either hardware or software, the interrupt will trigger again, even if the event that originally caused the interrupt did not occur again
- ◆ All interrupts are disabled after a system reset and enabled individually by software

Interrupt Summary

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Enable Flag	Priority Control
Reset	0000	Top	None	Always Enabled	Always Highest
External Interrupt 0 (/INT0)	0003	0	IE0 (TCON.1)	EX (IE.0)	PX0 (IP.0)
Timer 0 Overflow	000B	1	TF0 (TCON.5)	ET0 (IE.1)	PT0 (IP.1)
External Interrupt 1 (/INT1)	0013	2	IE1 (TCON.3)	EX1 (IE.2)	PX1 (IP.2)
Timer 1 Overflow	001B	3	TF1 (TCON.7)	ET1 (IE.3)	PT1 (IP.3)
UART0	0023	4	RI0 (SCON0.0) TI0 (SCON0.1)	ES0 (IE.4)	PS0 (IP.4)
Timer 2 Overflow	002B	5	TF2 (T2CON.7)	ET2 (IE.5)	PT2 (IP.5)
Serial Peripheral Interface	0033	6	SPIF (SPI0CN.7)	ESPI0 (EIE1.0)	PSPI0 (EIP1.0)
SMBus Interface	003B	7	SI (SMB0CN.3)	ESMB0 (EIE1.1)	PSMB0 (EIP1.1)
ADC0 Window Comparator	0043	8	AD0WINT (ADC0CN.2)	EWADC0 (EIE1.2)	PWADC0 (EIP1.2)

Interrupt Summary

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Enable Flag	Priority Control
Programmable Counter Array	004B	9	CF (PCA0CN.7) CCFn (PCA0CN.n)	EPCA0 (EIE1.3)	PPCA0 (EIP1.3)
Comparator 0 Falling Edge	0053	10	CP0FIF (CPT0CN.4)	ECP0F (EIE1.4)	PCP0F (EIP1.2)
Comparator 0 Rising Edge	005B	11	CP0RIF (CPT0CN.5)	ECP0R (EIE1.5)	PCP0R (EIP1.5)
Comparator 1 Falling Edge	0063	12	CP1FIF (CPT1CN.4)	ECP1F (EIE1.6)	PCP1F (EIP1.6)
Comparator 1 Rising Edge	006B	13	CP1RIF (CPT1CN.5)	ECP1R (EIE1.7)	PCP1R (EIP1.7)
Timer 3 Overflow	0073	14	TF3 (TMR3CN.7)	ET3 (EIE2.0)	PT3 (EIP2.0)
ADC0 End of Conversion	007B	15	AD0INT (ADC0CN.5)	EADC0 (EIE2.1)	PADC0 (EIP2.1)
Timer 4 Overflow	0083	16	TF4 (T4CON.7)	ET4 (EIE2.2)	PT4 (EIP2.2)
ADC1 End of Conversion	008B	17	AD1INT (ADC1CN.5)	EADC1 (EIE2.3)	PADC1 (EIP2.3)
External Interrupt 6	0093	18	IE6 (P3IF.6)	EX6 (EIE2.4)	PX6 (EIP2.4)
External Interrupt 7	009B	19	IE7 (P3IF.7)	EX7 (EIE2.5)	PX7 (EIP2.5)
UART1	00A3	20	RI1 (SCON1.0) TI1 (SCON1.1)	ES1 (EIE2.6)	PS1 (EIP2.6)
External Crystal OSC Ready	00AB	21	XTLVLD (OSCCN.7)	EXVLD (EIE2.7)	PXVLD (EIP2.7)

Interrupt Organization

- ◆ In the event of two or more simultaneous interrupts or an interrupt occurring while another is being serviced, there is both a fixed priority order and two programmable priority levels to schedule the interrupts

Enabling and Disabling Interrupts

- ◆ Each of the interrupt sources is individually enabled or disabled through the SFRs **IE**, **EIE1** and **EIE2**
- ◆ In addition to individual enable bits for each interrupt source, there is a global enable/disable bit, **EA (IE.7)** that is cleared to disable all interrupts or set to turn on all enabled interrupts
- ◆ Typically, two bits must be set to enable an interrupt:
 - the individual enable bit
 - the global enable bit
- ◆ Some interrupts need more than two bits to enable
- ◆ The RESET interrupt (interrupt 0) cannot be turned off, and always the highest priority

Programmable Interrupt Priority Levels

- ◆ Each interrupt source can be individually programmed to one of **two priority levels**, low or high, through an associated interrupt priority bit in the SFRs **IP**, **EIP1** and **EIP2**
- ◆ These three SFRs are cleared after a system reset to place all interrupts at low priority by default
- ◆ The two priority *levels* allow an ISR to be interrupted by an interrupt of higher priority than the current one being serviced
- ◆ A low priority ISR is pre-empted by a high priority interrupt
 - A high priority interrupt cannot be pre-empted.



Programmable Interrupt Priority Levels

- ◆ Having two priority levels is useful because some events require immediate action, while some other events can tolerate some delay in the response time
- ◆ Example: Radio Controlled (RC) Car
 - The current to the motor driving the wheels has to be adjusted periodically
 - This is done on a Timer overflow interrupt that is set to **high priority** because a delay in response can cause the motor to be damaged due to high current
 - Whenever user commands such as forward/reverse are received, the MCU has to take action
 - This can wait for a few extra milliseconds because that delay is small enough to be unnoticed by a user
 - This keypad interrupt is set to **low priority**

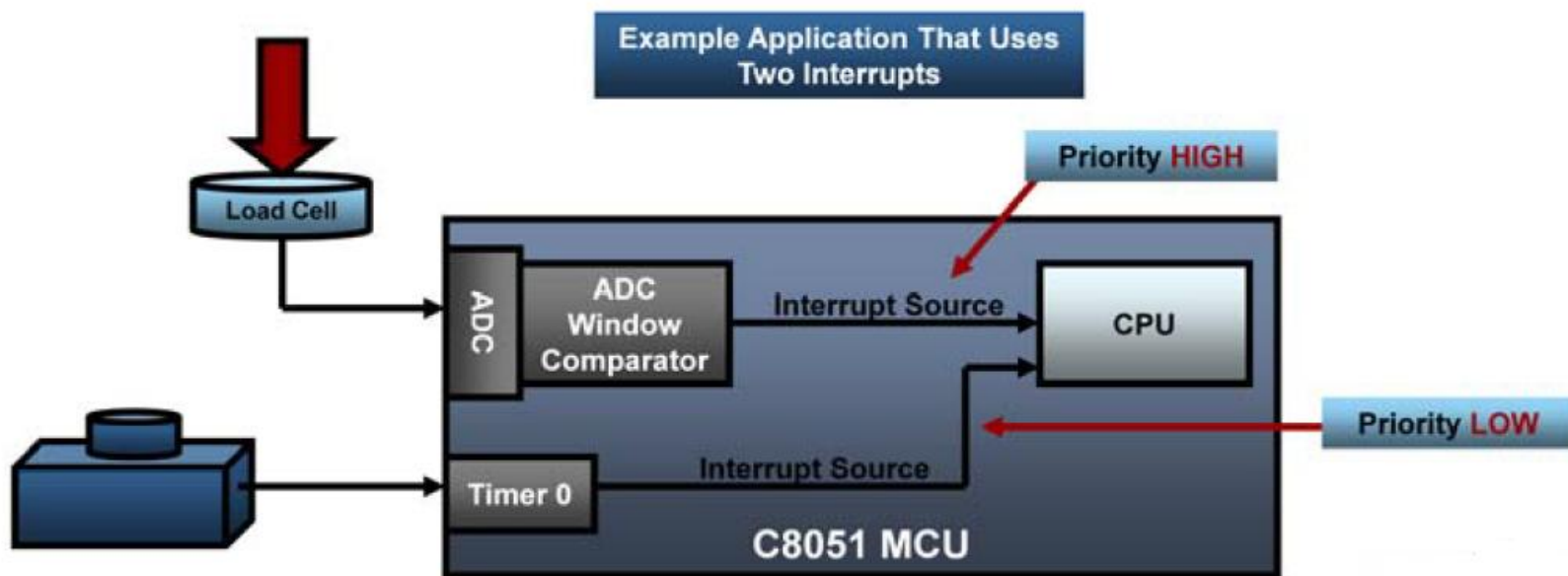
Fixed Priority Order

Interrupt Source	Interrupt Vector	Priority Order
Reset	0000	Top
External Interrupt 0 (/INT0)	0003	0
Timer 0 Overflow	000B	1
External Interrupt 1 (/INT1)	0013	2
Timer 1 Overflow	001B	3
UART0	0023	4
Timer 2 Overflow	002B	5
SPI 0	0033	6
SMBus Interface	003B	7
smaRTClock Alarm	0043	8
ADC0 Window Comparator	004B	9

- ◆ If two interrupts are recognized simultaneously, the interrupt with the higher priority **level** is serviced first
- ◆ If both interrupts have the same priority **level**, the fixed priority **order** determines which is serviced first
- ◆ Refer to *priority order column* in the Interrupt Summary table

Interrupt Priority Example

- ◆ High priority tasks: critical tasks
 - Safety critical systems
- ◆ Low priority tasks
 - Human user input
 - Display



Interrupt Pending Flags

- ◆ Some interrupt pending flags are automatically cleared by the hardware when the CPU vectors to the ISR
- ◆ **However, most are not cleared by the hardware, and must be cleared by software before returning from the ISR**
- ◆ If an interrupt pending flag remains set after the CPU completes the RETI instruction, a new interrupt request will be generated immediately and the CPU will re-enter the ISR after the completion of the next instruction
- ◆ If an interrupt is disabled, the interrupt pending flag is ignored by the hardware and program execution continues as normal

External Interrupts: /INT0 and /INT1

- ◆ Pins for the two external interrupt sources (/INT0 and /INT1) are allocated and assigned by the crossbar
- ◆ They are configured by bits IT0 (TCON.0) and IT1 (TCON.2)
- ◆ IE0 (TCON.1) and IE1 (TCON.3) serve as the interrupt-pending flags
- ◆ They are enabled using bits EX0 (IE.0) and EX1 (IE.1)
- ◆ The external interrupt sources can be programmed to be level-activated (low) or transition-activated (negative edge) on /INT0 or /INT1.
 - If a /INT0 or /INT1 external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by hardware when the CPU vectors to the ISR
 - When configured as level sensitive, the interrupt-pending flag follows the state of the external interrupt's input pin
 - The external interrupt source must hold the input active until the interrupt request is recognized
 - It must then deactivate the interrupt request before execution of the ISR completes, or else another interrupt request will be generated



TCON Register

Bit	Symbol	Description
7	TF1	Timer 1 Overflow Flag Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine (ISR). 0: No Timer 1 overflow detected 1: Timer 1 has overflowed
6	TR1	Timer 1 Run Control 0: Timer 1 disabled 1: Timer 1 enabled
5	TF0	Timer 0 Overflow Flag Same as TF1 but applies to Timer 0 instead. 0: No Timer 0 overflow detected 1: Timer 0 has overflowed
4	TR0	Timer 0 Run Control 0: Timer 0 disabled 1: Timer 0 enabled
3	IE1	External Interrupt 1 This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 ISR if IT1=1. This flag is the inverse of the /INT1 input signal's logic level when IT1=0
2	IT1	Interrupt 1 Type Select 0: /INT1 is level triggered 1: /INT1 is edge triggered
1	IE0	External Interrupt 0 Same as IE1 but applies to IT0 instead.
0	IT0	Interrupt 0 Type Select 0: /INT0 is level triggered 1: /INT0 is edge triggered

External Interrupts—Interrupt 6 and 7

- ◆ Port pins P3.6 and P3.7 can be used as inputs for the other 2 external interrupts—Interrupts 6 & 7
- ◆ They are edge-sensitive inputs and can be configured to trigger on a positive or negative edge
- ◆ The interrupt-pending flags and configuration bits for these interrupts are in the port 3 interrupt flag register (P3IF)
- ◆ When an active edge is detected on P3.6 or P3.7, the corresponding external interrupt flag (IE6 or IE7) will be set to logic 1 in the P3IF register
- ◆ If the associated interrupt is enabled, an interrupt will be generated and the CPU will vector to the associated interrupt vector location



External Interrupts—P3IF Register

Bit	Symbol	Description
7	IE7	<i>External Interrupt 7 Pending Flag</i> 0: No falling edge has been detected on P3.7 since this bit was last cleared. 1: This flag is set by hardware when a falling edge on P3.7 is detected.
6	IE6	<i>External Interrupt 6 Pending Flag</i> 0: No falling edge has been detected on P3.6 since this bit was last cleared. 1: This flag is set by hardware when a falling edge on P3.6 is detected.
5-4	-	UNUSED. Read = 00, Write = don't care
3	IE7CF	<i>External Interrupt 7 Edge Configuration</i> 0: External Interrupt 7 triggered by a falling edge on the IE7 input. 1: External Interrupt 7 triggered by a rising edge on the IE7 input.
2	IE6CF	<i>External Interrupt 6 Edge Configuration</i> 0: External Interrupt 6 triggered by a falling edge on the IE6 input. 1: External Interrupt 6 triggered by a rising edge on the IE6 input.
1-0	-	UNUSED. Read = 00, Write = don't care

IE—Interrupt Enable

Bit	Symbol	Description
7	EA	Enable All Interrupts 0: Disable all interrupt sources. 1: Enable each interrupt according to its individual mask setting.
6	IEGF0	General Purpose Flag 0 This is a general purpose flag for use under software control.
5	ET2	Enable Timer 2 Interrupt 0: Disable Timer 2 Interrupt. 1: Enable interrupt requests generated by TF2 (T2CON.7).
4	ES0	Enable UART0 Interrupt 0: Disable UART0 Interrupt. 1: Enable UART0 Interrupt.
3	ET1	Enable Timer 1 Interrupt 0: Disable Timer 1 Interrupt. 1: Enable interrupt requests generated by TF1 (TCON.7).
2	EX1	Enable External Interrupt 1 0: Disable external interrupt 1. 1: Enable interrupt request generated by the /INT1 pin.
1	ET0	Enable Timer 0 Interrupt 0: Disable Timer 0 Interrupt. 1: Enable interrupt requests generated by TF0 (TCON.5).
0	EX0	Enable External Interrupt 0 0: Disable external interrupt 0. 1: Enable interrupt request generated by the /INT0 pin.

EIE1—Extended Interrupt Enable 1

Bit	Symbol	Description
7	ECP1R	Enable Comparator1 (CP1) Rising Edge Interrupt 0: Disable CP1 Rising Edge interrupt. 1: Enable interrupt requests generated by CP1RIF (CPT1CN.5).
6	ECP1F	Enable Comparator1 (CP1) Falling Edge Interrupt 0: Disable CP1 Falling Edge interrupt. 1: Enable interrupt requests generated by CP1FIF (CPT1CN.4).
5	ECP0R	Enable Comparator0 (CP0) Rising Edge Interrupt 0: Disable CP0 Rising Edge interrupt. 1: Enable interrupt requests generated by CP0RIF (CPT0CN.5).
4	ECP0F	Enable Comparator0 (CP0) Falling Edge Interrupt 0: Disable CP0 Falling Edge interrupt. 1: Enable interrupt requests generated by CP0FIF (CPT0CN.4).
3	EPCA0	Enable Programmable Counter Array (PCA0) Interrupt 0: Disable all PCA0 interrupts. 1: Enable interrupt requests generated by PCA0.
2	EWADC0	Enable Window Comparison ADC0 Interrupt 0: Disable ADC0 Window Comparison Interrupt. 1: Enable Interrupt request generated by ADC0 Window Comparisons.
1	ESMB0	Enable System Management Bus (SMBus0) Interrupt 0: Disable all SMBus interrupts. 1: Enable interrupt requests generated by SI (SMB0CN.3).
0	ESPI0	Enable Serial Peripheral Interface (SPI0) Interrupt 0: Disable all SPI0 interrupts. 1: Enable interrupt requests generated by SPIF (SPI0CN.7).

EIE2—Extended Interrupt Enable 2

Bit	Symbol	Description
7	EXVLD	Enable External Clock Source Valid (XTLVLD) Interrupt 0: Disable XTLVLD interrupt. 1: Enable interrupt requests generated by XTLVLD(OXCXCN.7)
6	ES1	Enable UART1 Interrupt 0: Disable UART1 Interrupt. 1: Enable UART1 Interrupt.
5	EX7	Enable External Interrupt 7 0: Disable external interrupt 7. 1: Enable interrupt request generated by the External Interrupt 7 input pin.
4	EX6	Enable External Interrupt 6 0: Disable external interrupt 6. 1: Enable interrupt request generated by the External Interrupt 6 input pin.
3	EADC1	Enable ADC1 End of Conversion Interrupt 0: Disable ADC1 End of Conversion interrupt. 1: Enable interrupt requests generated by the ADC1 End of Conversion Interrupt.
2	ET4	Enable Timer 4 Interrupt 0: Disable Timer 4 Interrupt. 1: Enable interrupt requests generated by TF4 (T4CON.7).
1	EADC0	Enable ADC0 End of Conversion Interrupt 0: Disable ADC0 End of Conversion interrupt. 1: Enable interrupt requests generated by the ADC0 End of Conversion Interrupt.
0	ET3	Enable Timer 3 Interrupt 0: Disable Timer 3 Interrupt. 1: Enable interrupt requests generated by TF3 (TMR3CN.7).

IP—Interrupt Priority

Bit	Symbol	Description
7-6	-	UNUSED. Read=11, Write=don't care
5	PT2	Timer 2 Interrupt Priority Control 0: Timer 2 interrupt priority determined by default priority order. 1: Timer 2 interrupts set to high priority level.
4	PS0	UART0 Interrupt Priority Control 0: UART0 interrupt priority determined by default priority order. 1: UART0 interrupts set to high priority level.
3	PT1	Timer 1 Interrupt Priority Control 0: Timer 1 interrupt priority determined by default priority order. 1: Timer 1 interrupts set to high priority level.
2	PX1	External Interrupt 1 Priority Control 0: External Interrupt 1 interrupt priority determined by default priority order. 1: External Interrupt 1 interrupts set to high priority level.
1	PT0	Timer 0 Interrupt Priority Control 0: Timer 0 interrupt priority determined by default priority order. 1: Timer 0 interrupts set to high priority level.
0	PX0	External Interrupt 0 Priority Control 0: External Interrupt 0 priority determined by default priority order. 1: External Interrupt 0 set to high priority level.

EIP1—Extended Interrupt Priority 1

Bit	Symbol	Description
7	PCP1R	Comparator1 (CP1) Rising Interrupt Priority Control 0: CP1 Rising interrupt set to low priority level. 1: CP1 Rising interrupt set to high priority level.
6	PCP1F	Comparator1 (CP1) Falling Interrupt Priority Control 0: CP1 Falling interrupt set to low priority level. 1: CP1 Falling interrupt set to high priority level.
5	PCP0R	Comparator0 (CP0) Rising Interrupt Priority Control 0: CP0 Rising interrupt set to low priority level. 1: CP0 Rising interrupt set to high priority level.
4	PCP0F	Comparator0 (CP0) Falling Interrupt Priority Control 0: CP0 Falling interrupt set to low priority level. 1: CP0 Falling interrupt set to high priority level.
3	PPCA0	Programmable Counter Array (PCA0) Interrupt Priority Control 0: PCA0 interrupt set to low priority level. 1: PCA0 interrupt set to high priority level.
2	PWADC0	ADC0 Window Comparator Interrupt Priority Control 0: ADC0 Window interrupt set to low priority level. 1: ADC0 Window interrupt set to high priority level.
1	PSMB0	System Management Bus (SMBus0) Interrupt Priority Control 0: SMBus interrupt set to low priority level. 1: SMBus interrupt set to high priority level.
0	PSPi0	Serial Peripheral Interface (SPI0) Interrupt Priority Control 0: SPI0 interrupt set to low priority level. 1: SPI0 interrupt set to high priority level.

EIP2—Extended Interrupt Priority 2

Bit	Symbol	Description
7	PXVLD	External Clock Source Valid (XTLVLD) Interrupt Priority Control 0: XTLVLD interrupt set to low priority level. 1: XTLVLD interrupt set to high priority level.
6	EP1	UART1 Interrupt Priority Control 0: UART1 interrupt set to low priority level. 1: UART1 interrupt set to high priority level.
5	PX7	External Interrupt 7 Priority Control 0: External Interrupt 7 set to low priority level. 1: External Interrupt 7 set to high priority level.
4	PX6	External Interrupt 6 Priority Control 0: External Interrupt 6 set to low priority level. 1: External Interrupt 6 set to high priority level.
3	PADC1	ADC1 End of Conversion Interrupt Priority Control 0: ADC1 End of Conversion interrupt set to low priority level. 1: ADC1 End of Conversion interrupt set to high priority level.
2	PT4	Timer 4 Interrupt Priority Control 0: Timer 4 interrupt set to low priority level. 1: Timer 4 interrupt set to high priority level.
1	PADC0	ADC0 End of Conversion Interrupt Priority Control 0: ADC0 End of Conversion interrupt set to low priority level. 1: ADC0 End of Conversion interrupt set to high priority level.
0	PT3	Timer 3 Interrupt Priority Control 0: Timer 3 interrupt set to low priority level. 1: Timer 3 interrupt set to high priority level.



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